



# Digital Receiver Handbook: Basics of Software Radio

Fifth Edition

## Theory of Operation Applications Products

by

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## *Preface*

*Digital receivers have revolutionized electronic systems for a variety of applications including communications, data acquisition and signal processing.*

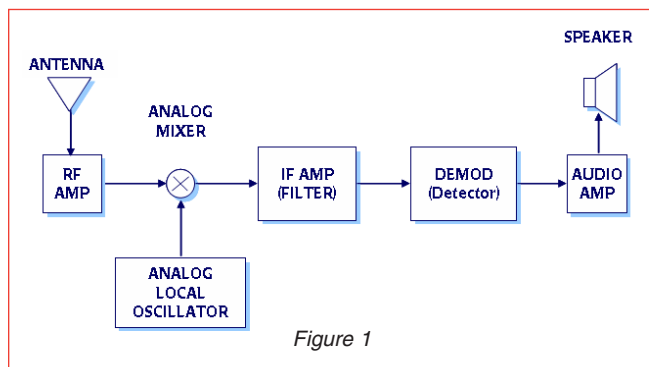
*This handbook shows how digital receivers, the fundamental building block for software radio, can replace conventional analog receiver designs, offering significant benefits in performance, density and cost.*

*In order to fully appreciate the benefits of digital receivers, a conventional analog receiver system will be compared to its digital receiver counterpart, highlighting similarities and differences.*

*The inner workings of the digital receiver will be explored with an in-depth description of the internal structure and the devices used. Finally, some actual receiver system implementations and available off-the-shelf board level digital receiver products for embedded systems will be described.*

## Theory of Operation

### Analog Receiver Block Diagram



The conventional heterodyne radio receiver, as seen in Figure 1, has been in use for nearly a century. Let's review the structure of the analog receiver so comparison to the digital receiver becomes apparent.

First the RF signal from the antenna is amplified, typically with a tuned RF stage, that amplifies a region of the frequency band of interest.

This amplified RF signal is then fed into a mixer stage. The other input to the mixer comes from the local oscillator whose frequency is controlled by the tuning knob on the radio.

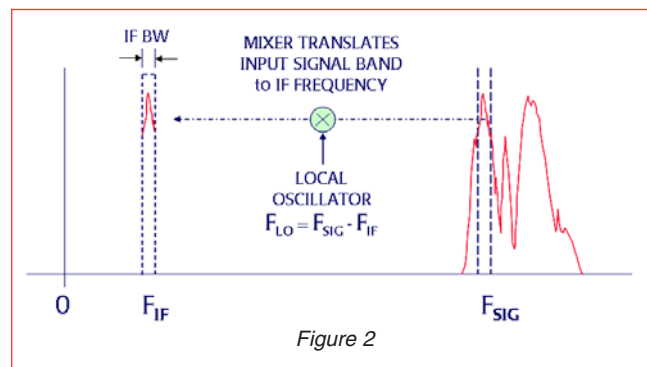
The mixer translates the desired input signal to the IF (Intermediate Frequency). See Figure 2.

The IF stage is a bandpass amplifier that only lets one signal or radio station through. Common center frequencies for IF stages are 455 kHz and 10.7 MHz for commercial AM and FM broadcasts.

The demodulator recovers the original modulating signal from the IF output using one of several different schemes.

For example, AM uses an envelope detector and FM uses a frequency discriminator. In a typical home radio, the demodulated output is fed to an audio amplifier which drives a speaker.

### Analog Receiver Mixing



The mixer performs an analog multiplication of the two inputs and generates a difference frequency signal.

The frequency of the local oscillator is set so that the difference between the local oscillator frequency and desired input signal (the radio station you want to receive) equals the IF.

For example, if you wanted to receive an FM station at 100.7 MHz and the IF is 10.7 MHz, you would tune the local oscillator to:

$$100.7 - 10.7 = 90 \text{ MHz}$$

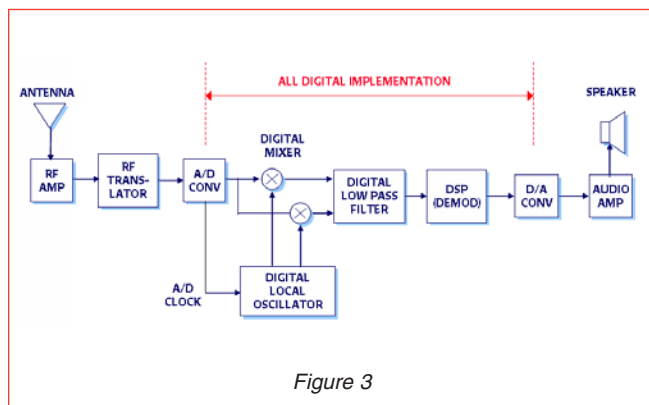
This is called “downconversion” or “translation” because a signal at a high frequency is shifted down to a lower frequency by the mixer.

The IF stage acts as a narrowband filter which only passes a “slice” of the translated RF input. The bandwidth of the IF stage is equal to the bandwidth of the signal (or the “radio station”) that you are trying to receive.

For commercial FM, the bandwidth is about 100 kHz and for AM it is about 5 kHz. This is consistent with channel spacings of 200 kHz and 10 kHz, respectively.

## Theory of Operation

### Digital Receiver Block Diagram



Take a look at the digital receiver block diagram shown in Figure 3. Note the strong similarity to the analog receiver diagram—all of the basic principles of analog receivers still apply.

Right after the RF amplifier and an optional RF translator stage, we use an A/D (analog-to-digital) converter to digitize the RF input into digital samples for the subsequent mixing, filtering and demodulation that are performed using digital signal processing elements.

Before we continue, let's first review a theorem fundamental to sampled data which lays the foundation for the A/D converter requirements.

#### Nyquist's Theorem:

*"Any signal can be represented by discrete samples if the sampling rate is at least twice the bandwidth of the signal."*

For example, if we use an A/D converter sampling at 70 MHz, then the bandwidth of the analog input must be less than 35 MHz.

Now let's see what happens if we ignore Nyquist's criterion.

### Aliasing

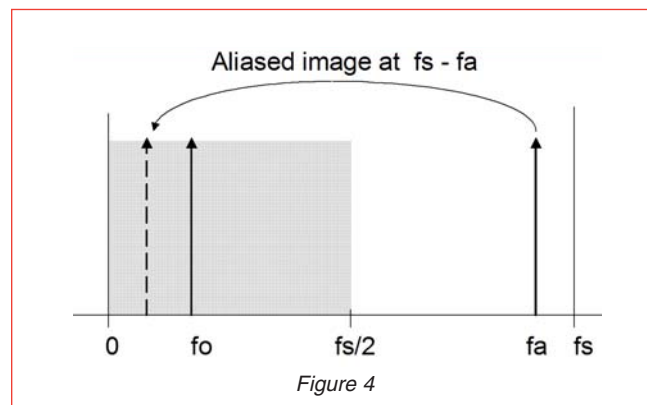


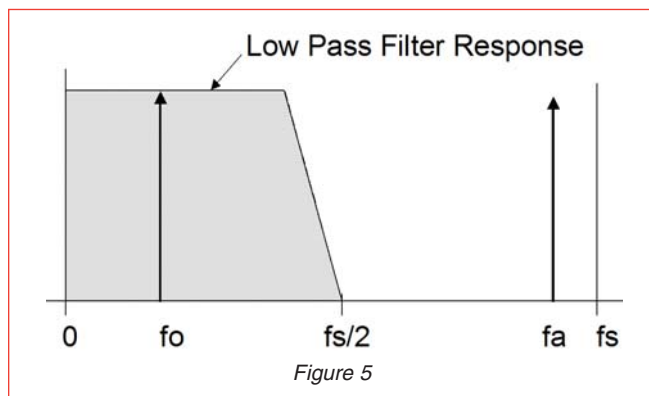
Figure 4 shows a frequency display of a system being sampled at frequency  $f_s$ . For all input signals below  $f_s/2$ , such as the one at  $f_0$ , we fully meet the Nyquist criterion. In fact, any number of signals can be present in the shaded region and all will be correctly represented in the sampled data.

But if we have a signal present at say,  $f_a$ , which is above  $f_s/2$ , the sampling process will generate an aliased image which will appear in the sampled data at  $f_s - f_a$ . This image cannot be distinguished from a true signal which might have been present at that same frequency.

The point is this: once an aliased image is created in the sampling process, no amount of further processing can distinguish between a true signal and an aliased signal. Therefore, it is imperative to prevent aliasing before it occurs.

## Theory of Operation

### Anti-Aliasing Filter



The most straightforward way to prevent aliasing is to use a low pass filter before the A/D converter which removes all signals above  $fs/2$ .

This filter, called an anti-aliasing filter, is seen in Figure 5. Now the signal at  $fa$  is blocked so the A/D converter never sees it.

Anti-aliasing filters are often included on the same board as the A/D converter as a convenience to the user.

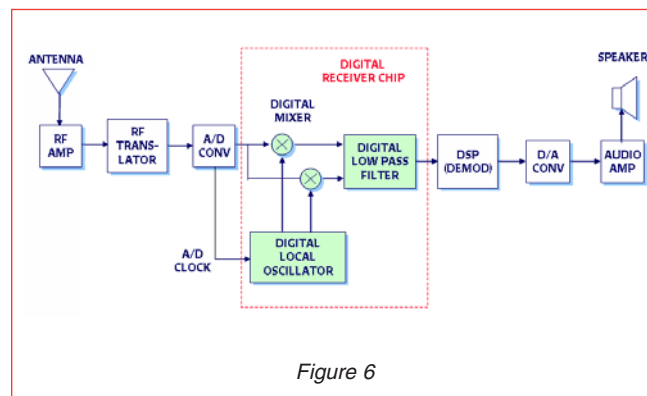
As a side note, Nyquist's criterion can also be met by limiting the bandwidth of the sampled signal using other types of filters.

For example, suppose we really wanted to receive signals between  $fs/2$  and  $fs$  in the above diagram. If we used a bandpass filter with a passband from  $fs/2$  to  $fs$ , we would fully meet the Nyquist criterion because the bandwidth is equal to one half the sampling rate.

Once the sampling is done, the band of signals from  $fs/2$  to  $fs$  is "folded" into the frequency band from DC to  $fs/2$ . This half-sampling frequency is often called the "folding frequency."

This technique is sometimes called "undersampling" and while this works well in theory, care must be taken in actual practice to ensure that the A/D converter supports the higher input frequencies it must handle.

### Digital Receiver Block Diagram



Looking again at the overall block diagram, the digital samples coming out of the A/D converter are being fed to the next stage which is the digital receiver chip—in the dotted line, as shown in Figure 6.

The digital receiver chip is typically contained on a single monolithic chip which forms the heart of the digital receiver system. It is also sometimes referred to as a digital downconverter (DDC) or a digital drop receiver (DDR).

Inside the digital receiver chip there are three major sections:

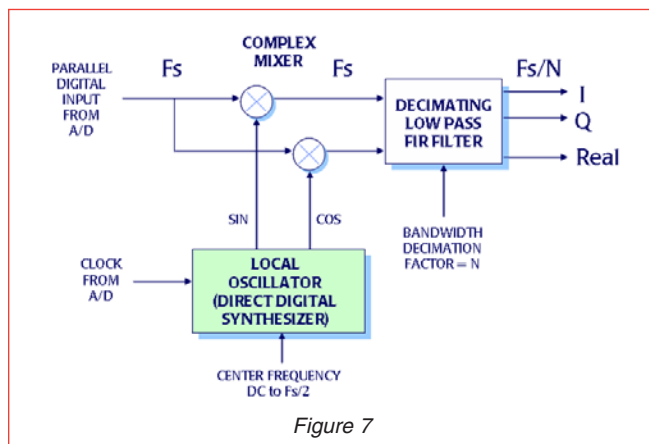
- Local Oscillator
- Mixer
- Decimating Low Pass Filter

Note that the inputs to the digital chip are the digital samples from the A/D and the A/D sample clock. With a 70 MHz A/D, samples are fed into this chip and processed in real time at rates up to 70 MHz!

We will now explore each section of the digital receiver system shown in Figure 6, starting with the digital local oscillator.

## Theory of Operation

### Local Oscillator



First, let's explore the Local Oscillator highlighted in Figure 7. It's a direct digital frequency synthesizer (DDS) sometimes called a numerically controlled oscillator (NCO). This device is implemented entirely with digital circuitry.

The oscillator generates digital samples of two sine waves precisely offset by 90 degrees in phase, creating sine and cosine signals. It uses a digital phase accumulator and sine/cosine lookup tables.

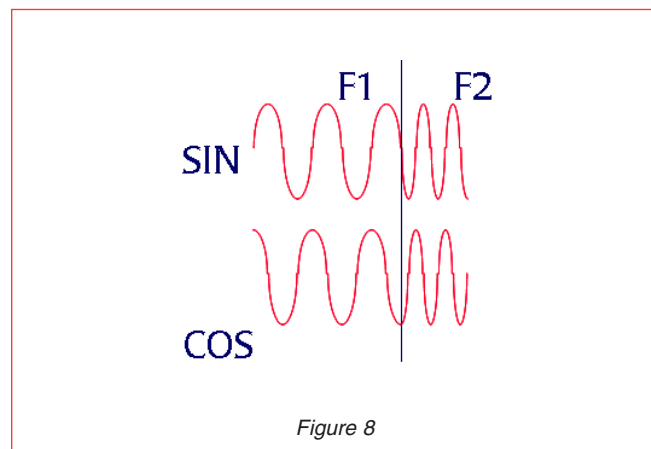
Note that the A/D clock is fed into the local oscillator. The digital samples out of the local oscillator are generated at a sampling frequency exactly equal to the A/D sample clock frequency,  $f_s$ .

*It is important to understand that the output sampling rate is always fixed at  $f_s$ , regardless of the frequency setting. The sine/cosine output frequency is changed by programming the amount of phase advance per sample.*

A small phase advance per sample corresponds to a low frequency and a large advance to a high frequency. The phase advance per sample is directly proportional to the output frequency and is programmable from DC to  $f_s/2$  with up to 32-bit of resolution.

Using a 70 MHz sampling clock, the frequency range is from DC to 35 MHz and the resolution is well below 1Hz.

### Phase Continuous Switching



The Local Oscillator has very impressive frequency switching characteristics as shown in Figure 8.

When switching between two frequencies, the digital accumulator precisely maintains the phase of the sine and cosine outputs for phase-continuous switching. When the frequency is changed, what actually changes is the amount of phase advance per sample.

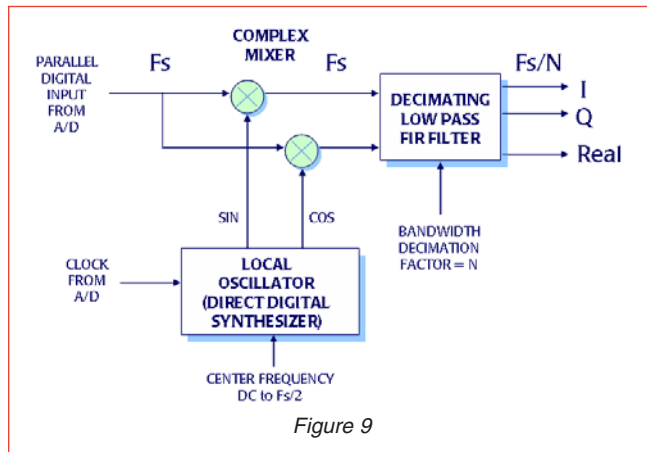
This allows the local oscillator to perform FSK (frequency shift keying) and very finely resolved sweeps. Transients and settling normally associated with other types of local oscillators, such as phase-locked loop synthesizers, are eliminated.

The time it takes to retune the local oscillator is simply the time it takes to load a new digital frequency word (32-bit binary number) into a register, usually well below one microsecond.

Some digital receiver chips employ a local oscillator with a built-in "chirp" function. This is a fast, programmable and precise frequency sweep which is very useful in radar systems.

## Theory of Operation

### Digital Mixer



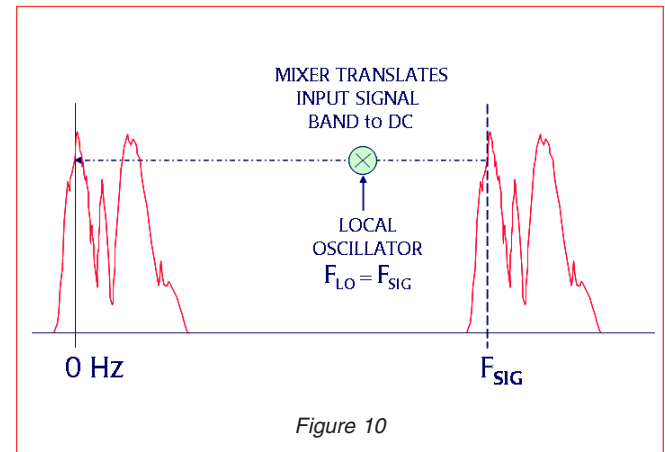
The next major component of the digital receiver chip is the Mixer seen in Figure 9. The Mixer actually consists of two digital multipliers. Digital input samples from the A/D are mathematically multiplied by the digital sine and cosine samples from the local oscillator.

Note that the input A/D data samples and the sine and cosine samples from the local oscillator are being generated at the same rate, namely, once every A/D sample clock. Since the data rates into both inputs of the mixers are the A/D sampling rate  $f_s$ , the multipliers also operate at that same rate and produce multiplied output product samples at  $f_s$ .

The sine and cosine inputs from the local oscillator create I and Q (in-phase and quadrature) outputs that are important for maintaining phase information contained in the input signal. From a signal standpoint, the mixing produces a single-sideband complex translation of the real input.

*Unlike analog mixers which also generate many unwanted mixer products, the digital mixer is nearly ideal and produces only two outputs: the sum and difference frequency signals.*

### Digital Receiver Mixer Translation



Let's look at the "difference" mixer product in the frequency domain as shown in Figure 10. At the output of the mixer, the high frequency wideband signals in the A/D input have been translated down to DC with a shift or offset equal to the local oscillator frequency.

This is similar to the analog receiver mixer except that the analog receiver mixes the RF input down to an IF (intermediate frequency).

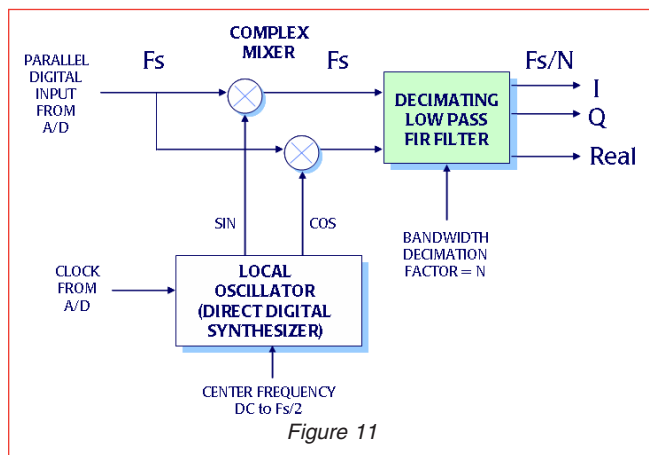
*In the digital receiver, the precision afforded by the digital signal processing allows us to mix right down to baseband (or 0 Hz). Overlapping mixer images, difficult to reduce with analog mixers, are strongly rejected by the accuracy of the sine and cosine local oscillator samples and the mathematical precision of the multipliers in the digital mixer.*

By tuning the local oscillator over its frequency range, any portion of the RF input signal can be translated down to DC. In effect, the wideband RF signal spectrum can be shifted around 0 Hz, left and right, simply by changing the local oscillator frequency.

The objective is to tune the local oscillator to center the signal of interest around 0 Hz so that the low pass filter that follows can pass only the signal of interest.

## Theory of Operation

### Decimating Low Pass Filter



Once the RF signal has been translated, it is now ready for filtering.

The decimating low pass filter accepts input samples from the mixer output at the full A/D sampling frequency  $f_s$ . It utilizes digital signal processing to implement an FIR (Finite Impulse Response) filter transfer function.

The filter passes all signals from 0 Hz up to a programmable cutoff frequency or bandwidth, and rejects all signals above that cutoff frequency.

This digital filter is a complex filter which processes both I and Q signals from the mixer. At the output you can select either I and Q (complex) values or just real values, depending on your system requirements.

### Decimating Filter Bandlimiting

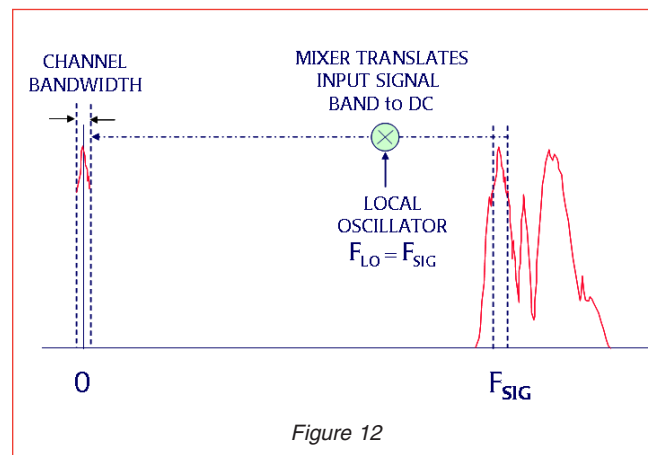


Figure 12 shows a representation of the action of the filter in the frequency domain. The filter passes only signals from 0 Hz up to the filter bandwidth. All higher frequencies have been removed.

Remember, the wideband input signal was translated down to DC by the mixer and positioned around 0 Hz by the tuning frequency of the local oscillator.

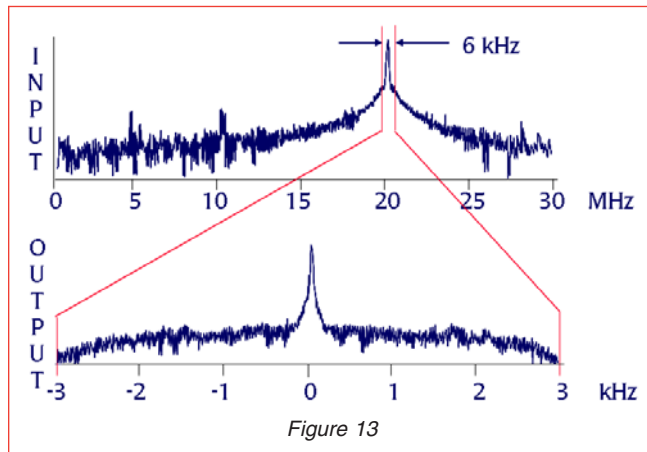
Now, at the filter output we have effectively selected a narrow slice of the RF input signal and translated it to DC. Note that we have blocked all other signals above and below the band of interest.

The bandlimiting action of the filter is analogous to the action of the IF stage in the analog receiver, except that the decimating low pass filter operates around DC instead of being centered at an IF frequency.



## Theory of Operation

### Frequency Zoom



As an example, take a look at an actual frequency display shown in Figure 13. The top figure shows a 30 MHz wideband RF input which was sampled by the A/D converter at 70 MHz.

Suppose we have a signal of interest at 20 MHz and we know that the bandwidth of the signal is 6 kHz.

By setting the local oscillator to 20 MHz and the bandwidth of the filter to 6 kHz we can translate the signal and extract only a 6 kHz band as shown in the bottom figure.

Note that the input band around 20 MHz has been translated down to DC and the complex output allows us to compute a complex FFT power spectrum centered at 0 Hz. Frequency components which were previously above 20 MHz are now to the right of 0 Hz and those below 20 MHz are to the left of 0 Hz. The 20 MHz carrier signal is now at 0 Hz exactly.

In this case, we have used the decimating low pass filter to perform a dramatic reduction in the signal bandwidth from 30 MHz down to 6 kHz. The sampling rate has also been reduced from 70 MHz to 7 kHz, a factor of 10,000!

Next, let's see exactly how to control the bandwidth of the FIR filter.

### Decimation Factor = N

$$\begin{aligned}\text{Output Bandwidth} &= \frac{\text{Input Sample Rate}}{N} \\ \text{Complex Output Sample Rate} &= \frac{\text{Input Sample Rate}}{N} \\ \text{Real Output Sample Rate} &= \frac{2 * \text{Input Sample Rate}}{N}\end{aligned}$$

Figure 14

In order to set the bandwidth of the filter, you need to program a parameter called the decimation factor as seen in Figure 14. Since the output bandwidth and the output sampling rate are directly related in the DDC, the decimation factor also sets the output sampling rate.

The decimation factor, N, determines the ratio between input and output sampling rates and also the ratio between input and output bandwidths. Note that the output sampling rate for real outputs is twice that for complex outputs.

For example, if you have an input sampling rate of 70 MHz and a desired nominal output bandwidth of 7 kHz, the decimation should be set for 10,000. The output sampling rate would be 7 kHz for complex outputs and 14 kHz for real outputs.

Note that the usable bandwidth is always less than the Nyquist bandwidth, hence in the previous example we see a real input bandwidth of about 30 MHz (with a 70 MHz sampling rate) and an output bandwidth of about 6 kHz (with a complex output sampling rate of 7 kHz or a 14 kHz output for real).

Digital receivers can be divided into two classes, *narrowband* and *wideband*, distinguished by the programmable range of decimation factors.

*Narrowband* receivers typically have a range of decimation factors from 32 or 64 to 65,536 or 131,072, depending on the chip manufacturer.

*Wideband* receivers typically have a range of decimation factors from 2 to 64.

## Theory of Operation

### FPGA Implementation of Digital Receivers

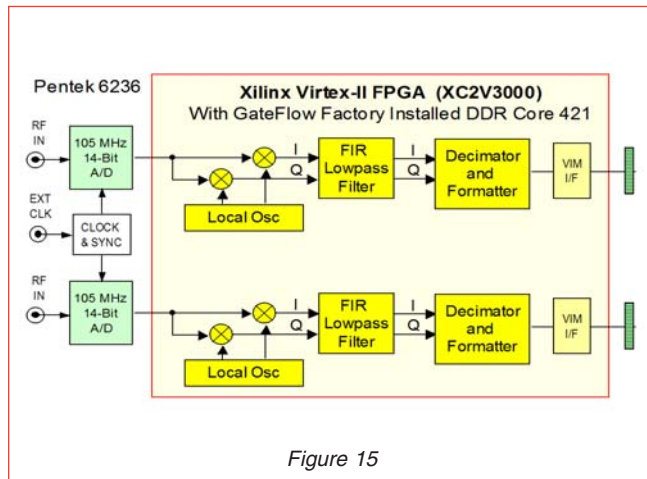


Figure 15

FPGAs (Field Programmable Gate Arrays) have become more appropriate for implementing digital receiver functions because of the built-in hardware multipliers and generous RAM. Remember that the digital mixer section is nothing more than a hardware multiplier. The FIR filter also uses one multiplier for each filter tap plus RAM for delay memory.

The Pentek GateFlow® IP Core Library for software radio includes fast FFT engines, radar pulse compressors, and digital receivers. These cores allow FPGA designers to readily incorporate these highly optimized functions in FPGA-based products.

Most of Pentek's recent software radio products include user-configurable FPGAs in the signal path to support IP cores and custom DSP algorithms. Pentek also offers factory installation of IP cores in several of these products, thereby eliminating the FPGA design effort and allowing customers to easily take advantage of this exciting new technology.

Figure 15 above shows a dual channel A/D converter VIM-2 module with the Pentek GateFlow Wideband Receiver Core 421 installed. This core replaces the TI / GC1012B chip and offers higher dynamic range and user-programmable FIR coefficients. It accepts 16-bit inputs instead of the 12-bit inputs of the ASIC to take full advantage of the 14-bit A/D converters. For the latest FPGA offerings visit the online FPGA Resource at [pentek.com/gateflow](http://pentek.com/gateflow).

### FPGAs Tackle DSP Functions

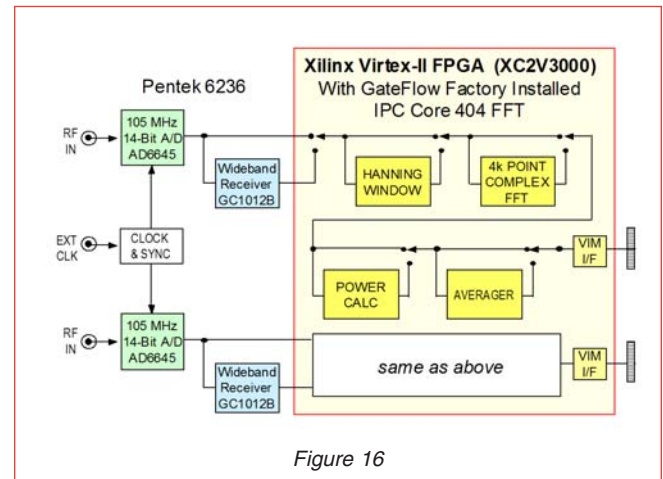


Figure 16

FPGAs not only offer significant advantages as specialized replacements for standard ASIC digital receivers, they also provide extremely high performance signal processing capabilities to offload these tasks from DSP and RISC processors.

An example is the Pentek GateFlow IP Core 404 4k-point complex FFT. Although all GateFlow IP Cores are designed for use on any Virtex-II, Virtex-II Pro or Spartan 3 product, the Core 404 is available as a factory installed option on the Model 6236 Dual Channel Receiver VIM-2 module shown in Figure 16.

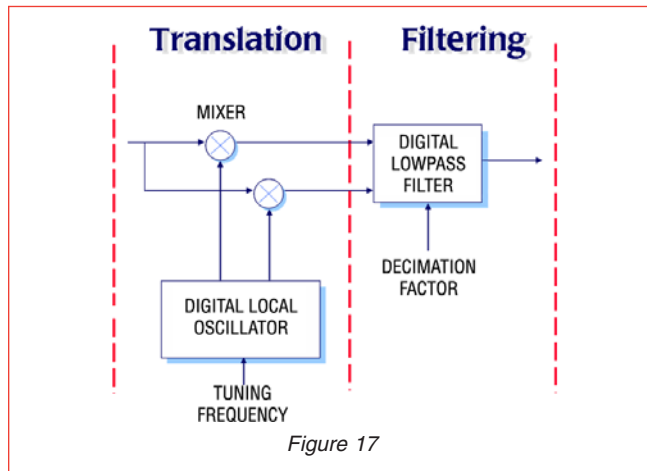
In this case, real data from the A/D converter or complex I and Q samples from the wideband digital receiver can be directed into the FFT engine. The first stage performs an optional Hanning (or other) windowing function as a preprocessing step before the complex 4k-point FFT.

The output of the FFT can be optionally converted to power by summing  $I^2$  and  $Q^2$ . Finally, consecutive outputs can be optionally averaged to reduce wideband noise.

Because of the highly-parallel architecture of this IP Core, it can sustain real time input sampling rates of up to 160 MHz. It would take approximately eight G4 PowerPCs running at 1 GHz to equal the processing power of this impressive engine!

## Theory of Operation

### Two-Step Signal Processing



To review, the digital receiver chip performs two major signal processing operations controlled by two programmable parameters (Figure 17):

- 1) Translation of the input signal down to DC is controlled by setting the tuning frequency of the local oscillator.
- 2) Low pass filtering bandwidth and output sampling rate are both controlled by setting the decimation factor.

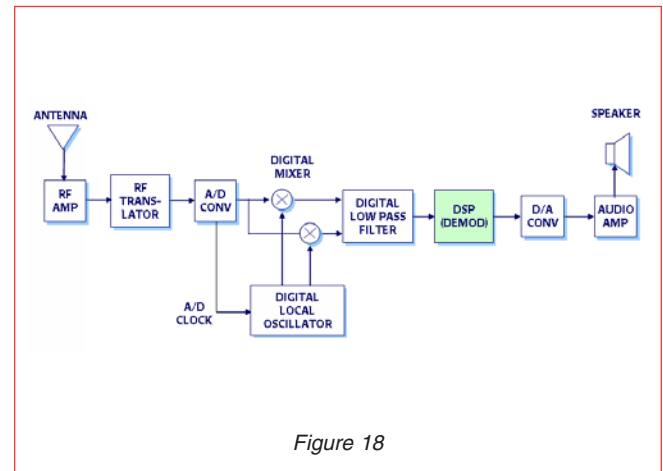
Because everything inside the decimating low pass filter is performed with digital circuitry and DSP techniques, there are no undesirable effects normally associated with conventional analog filters.

There are no initial component tolerance or temperature variations or aging characteristics. No calibration or preventive maintenance is required. This provides excellent channel-to-channel matching for applications where phase variation between channels is important, such as direction finding.

The FIR digital filters used have linear phase for well-behaved transient response. The filter bandwidth is programmable over a wide range (1000 to 1), with absolutely predictable and uniform response throughout.

Lastly, the signal is tailored precisely for DSP processing by preselecting only the signal of interest through bandlimiting and providing it to the DSP at the optimum sampling rate.

### Digital Receiver Block Diagram



Returning to our overall digital receiver block diagram shown in Figure 18, our output signal is now translated, filtered and bandlimited and is ready for further processing.

Note that the output signal from the decimating low pass filter is still a sampled time signal which could represent any kind of modulated or unmodulated signal. We could send this signal directly to a D/A converter, producing an analog waveform.

For straight single-sideband frequency division multiplexed speech, for example, we could now connect the D/A output to a speaker and listen to the selected voice channel directly.

In many systems, further processing is required, as with modem demodulation for example. Since the output of the digital receiver is now at a much lower sampling rate than the original wideband input signal, this additional modem processing can now be readily handled by a DSP or an FPGA.

## Theory of Operation

### DSP Demodulation Functions

- Frequency and Phase Shift Keying (FSK, PSK)
- AM, FM, and PM
- Spread Spectrum
- Custom Frequency Agile Schemes
- Signal Analysis (FFT's), Signal Identification
- Signal Recording and Tracking

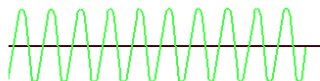


Figure 19

Virtually any form of demodulation can be implemented just by loading the DSP or FPGA with the appropriate algorithm (Figure 19). AM can be demodulated with an envelope detector, FM & PM can be demodulated using a phase or frequency discriminator algorithm.

The ability to quickly change the local oscillator allows frequency-agile modulation schemes to be accommodated as well. Analysis functions include energy detection such as required by scanning receivers that may be implemented with an FFT, for example.

Other analysis functions include cryptography, identification of transmitters based on transmission frequency, modulation schemes, and other signal characteristics.

Once the signal is successfully brought into the DSP arena, automated functions such as center frequency and bandwidth tuning can be implemented to track a complex signal which may be moving or hopping. Interesting signals can be stored on hard disk, tape or other media and the time of the signal event can be logged as well.

*With this arrangement, when new or proprietary demodulation, processing, or analysis schemes are required, no new hardware is necessary. Instead, a new DSP software algorithm is loaded.*

### Key Benefits of Digital Receivers

- Dedicated digital receiver hardware preselects only signals of interest
- Saves significant DSP horsepower since DSP requirements are directly proportional to sampling rate

Figure 20

Think of the digital receiver as a hardware preprocessor for DSP. It preselects only the signals you are interested in and removes all others. This provides an optimum bandwidth and minimum sampling rate into the DSP.

Since the number of DSPs required in a system is directly proportional to the sampling rate of input data, by reducing the sampling rate you can dramatically reduce the cost and complexity of the DSP system that follows.

Even if the digital receiver outputs do not require a great deal of signal processing, reduction of bandwidth and sampling rate helps save time in data transfers to another subsystem, helps minimize recording time and tape or disk space, and speeds up communication channels.

## Theory of Operation

### Digital Receiver Chip Performance

|                       | Narrowband      |                    |                          |                   |                      |                       | Wideband             |                              |                       |
|-----------------------|-----------------|--------------------|--------------------------|-------------------|----------------------|-----------------------|----------------------|------------------------------|-----------------------|
|                       | TI / GC<br>4014 | Intersil<br>50214B | TI / GC<br>1011A         | Intersil<br>50016 | TI / GC<br>4016      | Pentek IP<br>Core 430 | TI / GC<br>1012A / B | Pentek IP<br>Core 421        | Pentek IP<br>Core 422 |
| No of Channels        | 4               | 1                  | 1                        | 1                 | 4                    | 256                   | 1                    | 1                            | 1                     |
| Sample Freq ( $f_s$ ) | 62.5 MHz        | 65 MHz             | 70 MHz                   | 75 MHz            | 100 MHz              | 185 MHz               | 80 / 100 MHz         | 160 MHz                      | 296 MHz               |
| Input bits            | 14/16           | 16                 | 12                       | 16                | 14/16                | 16                    | 12                   | 16                           | 16                    |
| Min Decim (N)         | 32              | 2                  | 64                       | 64                | 32                   | 1024                  | 2, 4, 8              | 2, 4, 8                      | 2, 4, 8               |
| Max Decim (N)         | 65k             | 65k                | 65k                      | 131k              | 16k                  | 9984                  | 16, 32, 64           | 16, 32, 64                   | 16, 32, 64            |
| Resampler             | No              | Yes                | No                       | No                | Yes                  | No                    | No                   | No                           | No                    |
| Custom FIR            | Yes             | Yes                | No                       | No                | Yes                  | Yes                   | No                   | Yes                          | Yes                   |
| 3 dB Output BW        | Prog            | Prog               | $0.8f_s/N$<br>$0.9f_s/N$ | $0.56f_s/N$       | Prog                 | Prog                  | $0.8f_s/N$           | Prog                         | Prog                  |
| VME Boards            |                 |                    |                          |                   |                      |                       |                      | 6821<br>6822                 | 6821<br>6822          |
| VIM Modules           |                 |                    |                          |                   | 6230<br>6231<br>6232 |                       | 6235<br>6236         | 6235<br>6236<br>6250<br>6251 | 6250<br>6251          |
| PMC Modules           |                 |                    |                          |                   | 7131<br>7140         | 7140                  |                      |                              |                       |
| PCI Boards            |                 |                    |                          |                   | 7631<br>7640         | 7640                  |                      |                              |                       |
| cPCI Boards           |                 |                    |                          |                   | 7231<br>7240         | 7240                  |                      |                              |                       |

The above chart shows the salient characteristics for seven popular digital receiver chips and three FPGA IP cores. Note that the range of decimation settings for the narrowband chips on the left is much higher than for the wideband receivers on the right. The output sampling frequencies for real and complex outputs are shown as a function of the decimation factor N.

Notice also that the 3 dB output bandwidth of the FIR filter is expressed as a percentage of the input sampling rate divided by N. This percentage reflects the frequency characteristics of the specific FIR filter function implemented in the digital receiver chip. Each filter characteristic has its own passband flatness, rolloff rate, and stop band attenuation characteristics suitable for different applications.

As an example, if we were using the TI/GC1011A with a 64 MHz A/D converter and needed a usable output bandwidth of 10 kHz, we could solve for the appropriate decimation factor setting as follows:

$$10 \text{ kHz} = 0.80 \cdot f_s / N \quad \text{or} \\ N = 0.80 \cdot 64 \text{ MHz} / 10 \text{ kHz} = 5120$$

Note that the decimation factors of narrowband receivers are programmable in steps of 1 or 4 and the wideband receivers are programmable in binary steps as shown. Some receivers allow entry of custom FIR filter coefficients and others have output resampling stages to support custom filter characteristics and output sampling rates.

Model numbers of Pentek products using each type of digital receiver are shown at the bottom.

## Applications

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### Applications of Digital Receivers

- Tracking Receiver System
- Signal Intelligence Receiver
- Direction Finding System
- Radar Signal Processing System
- Wireless Cellular Development System

Digital receivers can be used in many different systems:

Tracking receivers and signal intelligence receivers can be highly automated because digital receivers allow DSPs to perform the signal identification and analysis functions as well as the adaptable tuning functions.

Direction finding is an ideal application for digital receivers because of their excellent channel-to-channel phase matching and consistent delay characteristics.

Radar applications benefit from the tight coupling of the A/D, digital receiver and DSP functions to process wideband signals. FPGAs are especially well suited to handle FFT and pulse compression tasks normally required in the signal processing sections.

Some of the digital receiver chips employ special features like a “chirp” sweep generator function in the local oscillator, ideal for high-performance radar applications.

Cellular phone applications are one of the strongest high-volume applications because of the high density of tightly-packed frequency division multiplexed voice channels.

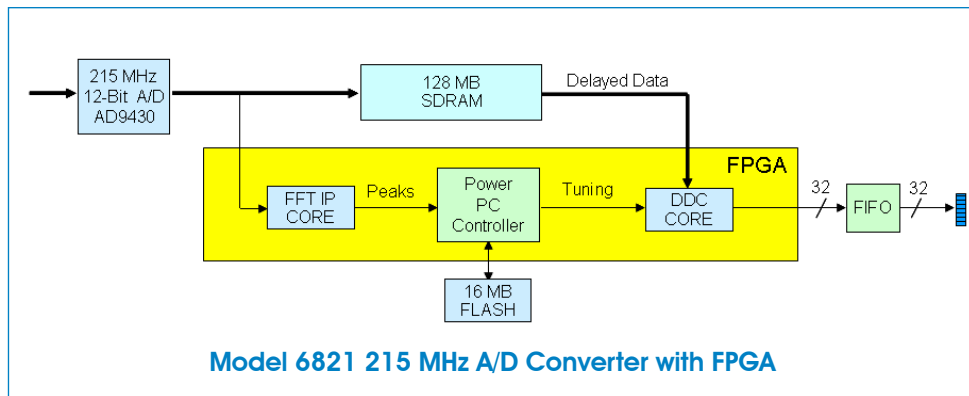
As a general capability, any system requiring a tunable bandpass filter should be considered a candidate for using digital receivers. Take a look at the following application examples to give you some more details.

Product overviews of all models described in the applications section are included in the last section of the handbook.



## Applications

### Tracking Receiver System



#### System Highlights

- A/D data delivered into SDRAM that acts as a digital delay memory
- A/D data also delivered into a Pentek FFT IP core in FPGA
- FFT core detects the strength of signals at each analysis frequency
- PowerPC controller in FPGA sorts signals according to peak strength
- PowerPC controller also tunes DDC IP core in FPGA to the strongest signal frequencies
- Delayed data from SDRAM feeds DDC IP core to compensate for FFT calculation time
- DDC captures these moving signals in real time and downconverts them to baseband



Model 6821 commercial (left) and conduction-cooled version

Figure 21

A tracking receiver locates unknown signals, locks onto them and tracks them if their frequency changes.

As shown in Figure 21, to implement this receiver, we use the 128 MB SDRAM of the Model 6821 to create a delay memory function.

Samples from the A/D are sent into a circular buffer within the SDRAM and also to a Pentek FFT IP core implemented in the FPGA. The spectral peaks of the FFT indicate the frequencies of signals of interest present at the input.

The PowerPC microcontroller of the FPGA digests this frequency list and decides which signals to track. It then tunes the Pentek DDC core, also implemented in

the FPGA, accordingly. The delayed data from the circular buffer feeds the input of this DDC core.

The digital delay can be set to match the time it takes for the FFT energy detection and the processor algorithm for the tuning frequency decision, so that frequency-agile or transient signals can be recovered from their onset. The dehopped baseband output is delivered to the rest of the system through the FPDP port or, optionally, across a VXS link.

See page 22 for a more detailed description of the Pentek Model 6821 A/D Converter. This Model is also available in a dual-channel version as Model 6822, see page 23. Both Models are available in commercial and conduction-cooled versions.

## Applications

### 32-Channel Signal Intelligence Receiver

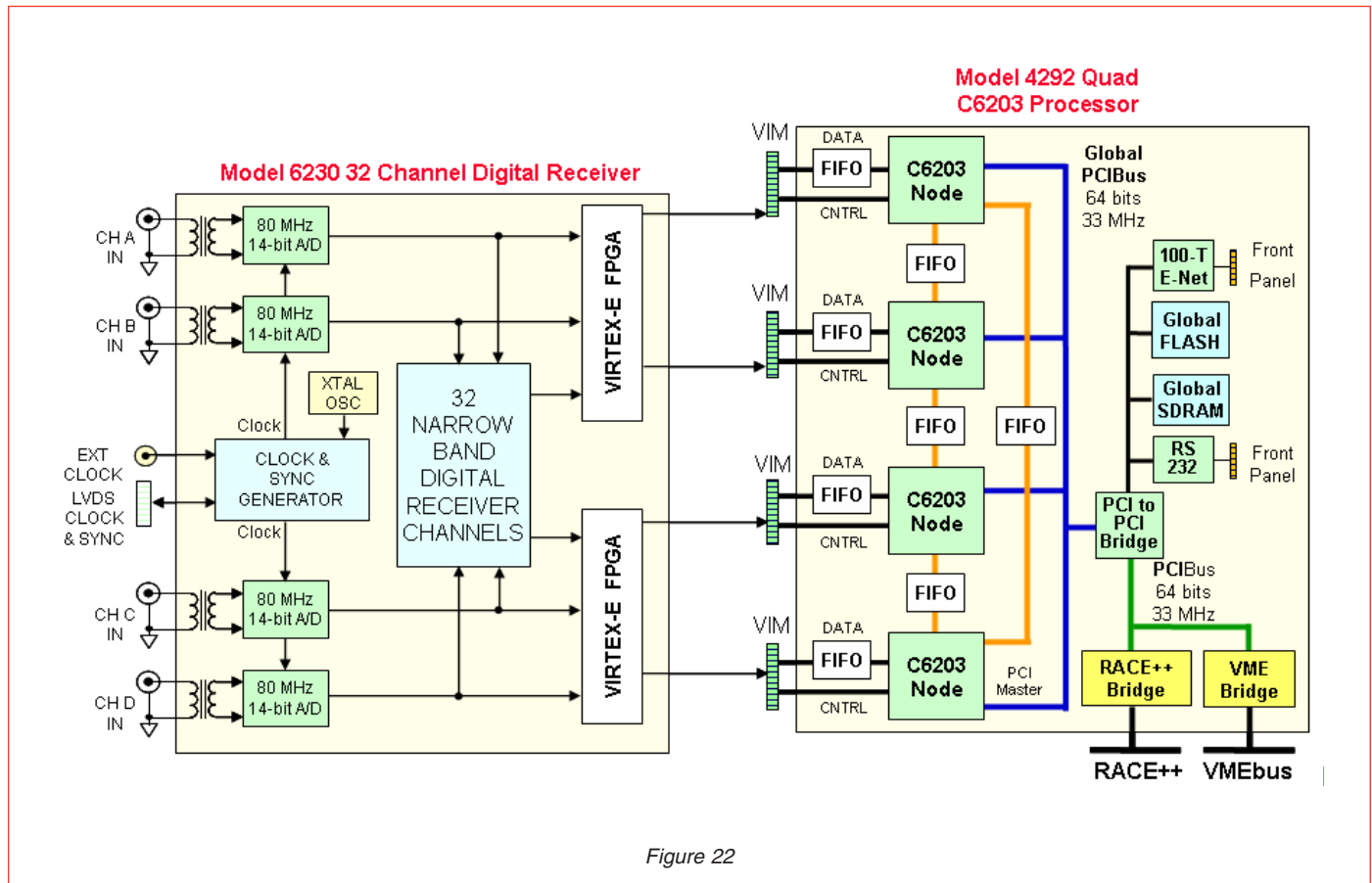


Figure 22

This compact receiver system incorporates the entire signal processing chain from the A/D converters through digital downconversion and filtering, to decoding, demodulation and analysis performed by FPGAs and PowerPC's. And it all fits in just a single VMEbus slot!

The Model 6230, a 32-Channel Narrowband Receiver, is a VIM-4 mezzanine module that includes four 14-bit A/D converters operating at sampling rates up to 80 MHz. All four A/D outputs are delivered to eight 4-channel receiver chips so that each of the 32 narrowband channels can independently select any one of the four A/D converters as the input source.

The 32 narrowband receiver outputs are sent into two FPGAs where channel selection and data formatting take place prior to sending the data across the VIM interface to the quad C6203 board. Note that the wideband A/D outputs are also delivered directly to the FPGAs, so they are also available for transfer to the processor board.

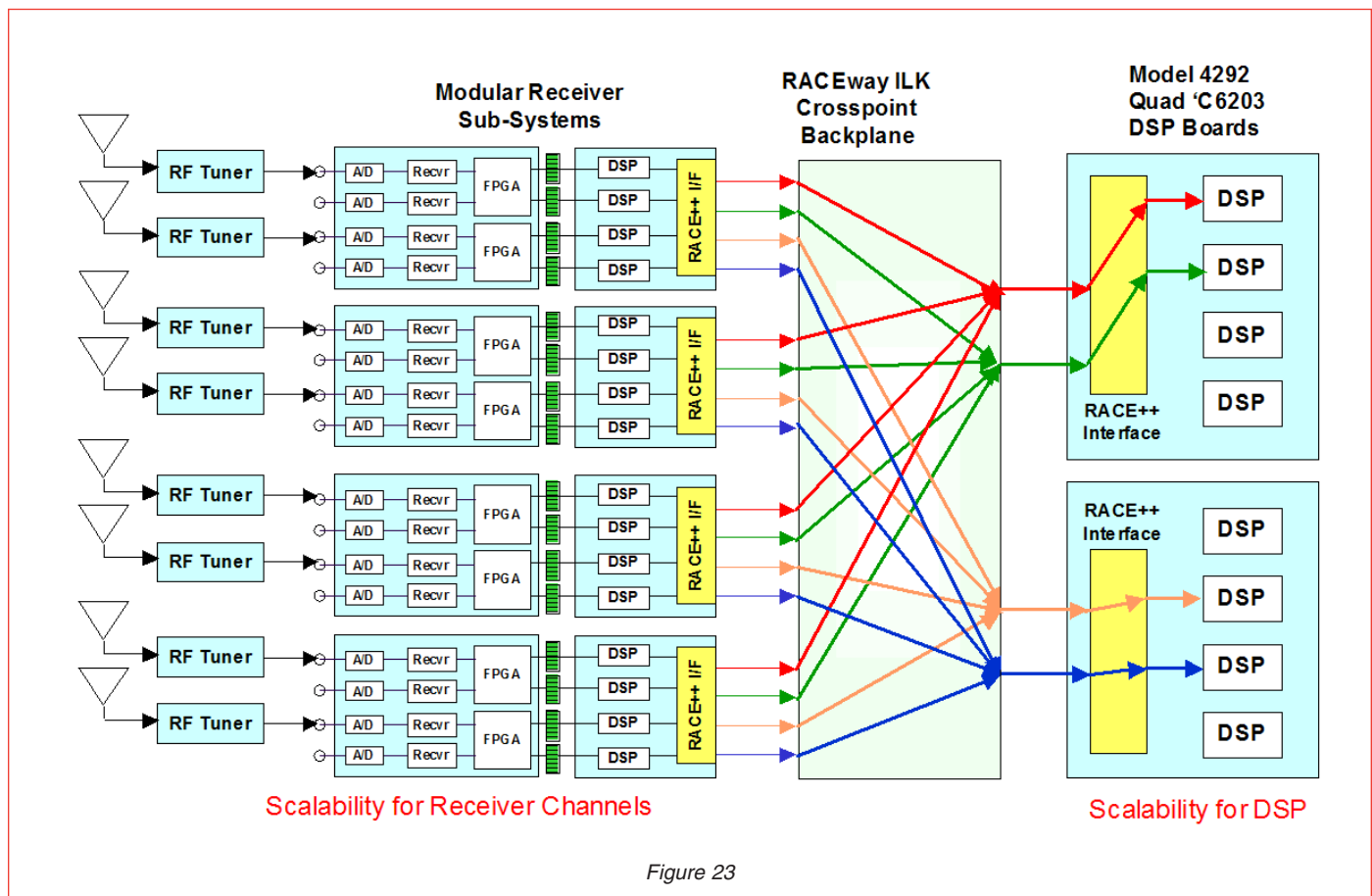
Custom algorithms may be incorporated in the FPGAs to support decoding, demodulation and other signal processing tasks, thus off-loading the processor.

Because of its modular, single-board design, this system is highly scalable to support low-cost, high-density systems with hundreds of channels in a relatively small space.



## Applications

### Direction Finding System



In this direction finding application, we need to route digitized signals from eight antennas into a DSP which compares the arrival time and phase of each signal. This allows the DSP to compute the location, speed and direction of travel of a mobile radio source.

Four of the 32-channel narrowband receiver sub-systems shown on the previous page (Figure 22) are driven by eight antennas. Two of the 32 channels in each subsystem are tuned to the frequency of a source transmitter. This way, eight different versions of the same transmitted signal are acquired, one from each antenna. The data samples are time stamped, organized in packets and then sent out over RACEway, a high-performance industry standard backplane fabric. RACEway allows simultaneous high-speed data transfers between pairs of boards. Even though data is sent in

packets, the output samples are fully buffered so no data is lost.

Each RACEway packet contains a header which includes channel identification, signal arrival time, and routing instructions to a destination DSP address. Each of the eight packets for a single source are directed to one of the DSPs, where phase and arrival time beam-forming calculations are performed. This highly scalable system supports continuous simultaneous tracking of up to sixteen targets.

By simply changing the RACEway packet routing addresses through software, you can completely reconfigure your system and assign any number of channels to any number of DSPs. Routing information can be allocated dynamically during runtime to accommodate changing conditions.

## Applications

### Radar Signal Processing System

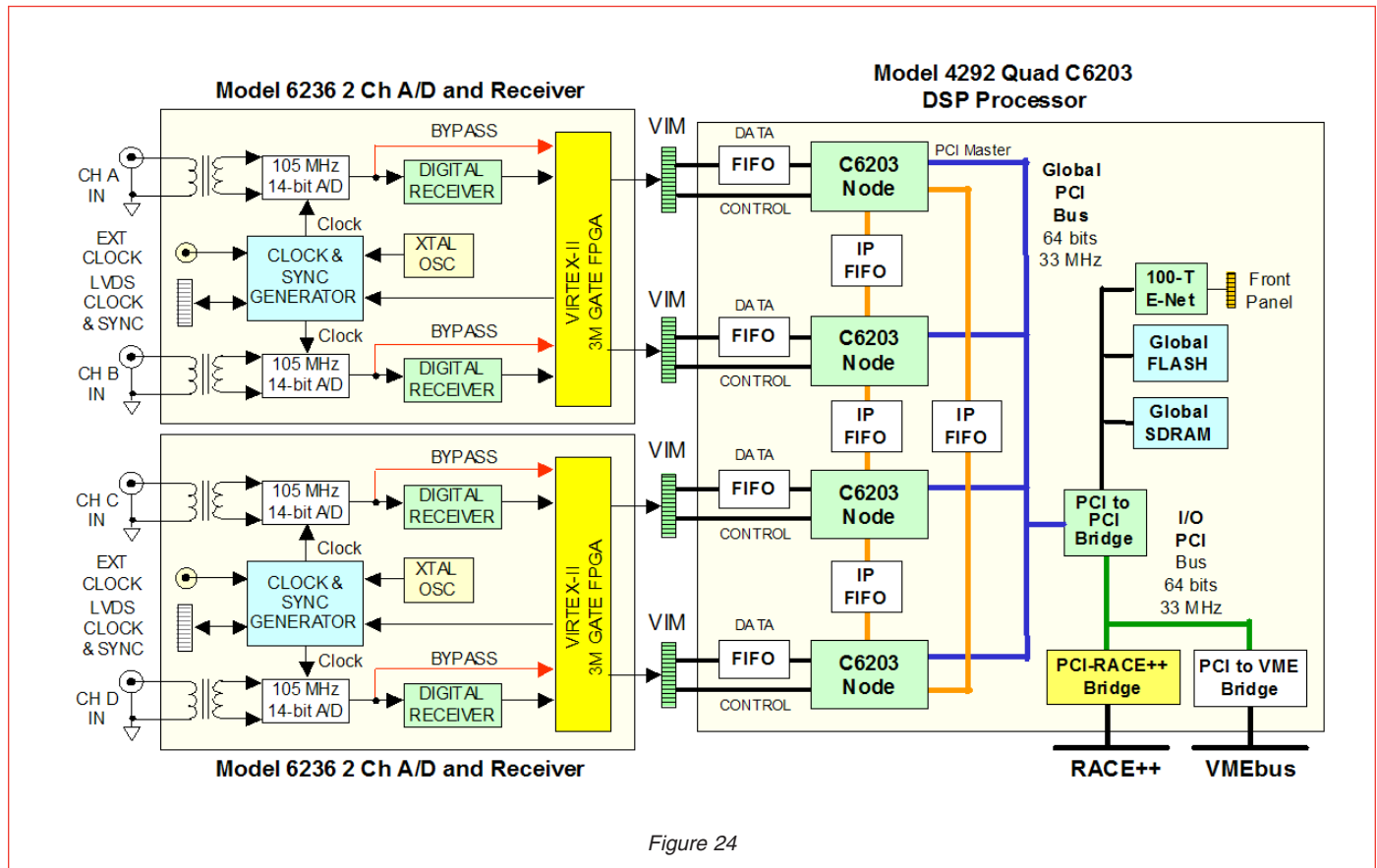


Figure 24

Radar is well served by high-speed A/D converters and wideband digital receivers. The channelized system shown in Figure 24, takes advantage of two Model 6236 Wideband Receiver VIM-2 mezzanine modules mounted on the Model 4292 Quad C6203 DSP processor.

Operating at a sampling rate of up to 100 MHz, the A/D converters can digitize baseband signals with bandwidths up to 45 MHz. After frequency translation and filtering, the receivers deliver complex (I & Q) data into the Virtex-II FPGAs. Here, data may be processed by custom user-defined algorithms before it is sent across the VIM interface to the DSPs.

Note that the wideband A/D outputs are also connected directly to the FPGAs, either for delivery to the DSPs or for internal processing tasks.

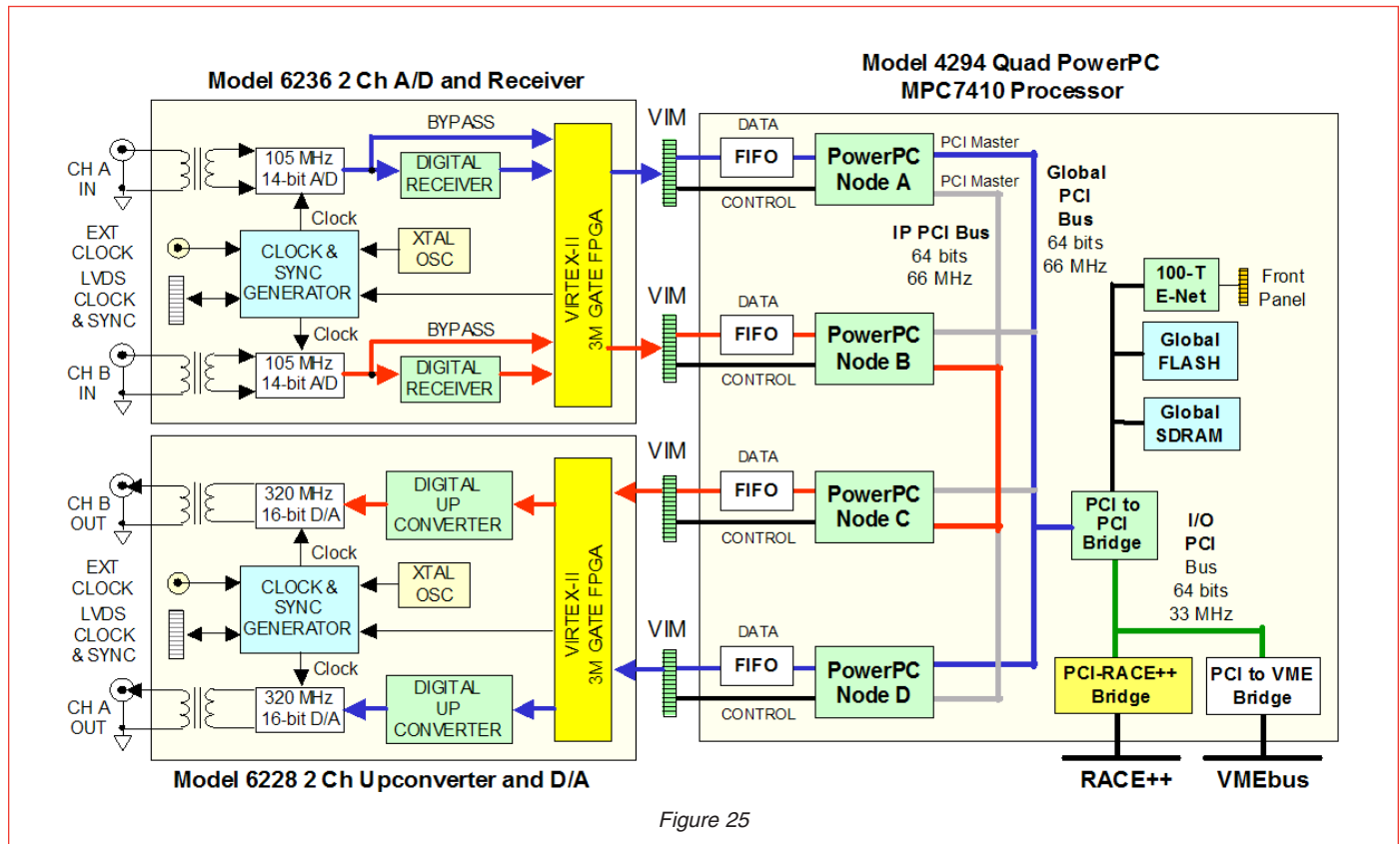
The optional GateFlow FPGA Design Kit and IP Core Libraries support custom signal processing algorithms. Factory installed IP cores available for the Model 6236 include Core 421 Wideband Receiver, Cores 401 and 404 FFTs, and Core 440 Pulse Compressor. Gating and triggering signals are accepted on front panel connectors of the 6236 to capture transient signals.

Supporting peak data transfer rates up to 100 MHz to each of the four processing nodes, the VIM interface eliminates the bottlenecks normally associated with traditional system interconnect schemes.

An optional RACE++ (enhanced RACEway) interface is available for delivering output data from all four processing nodes to downstream memory, storage, or array processors at transfer rates up to 267 MB/sec.

## Applications

### Wireless Cellular Development System



Next generation wireless standards require increasingly wider bandwidths to support the latest spread spectrum techniques. The system shown in Figure 25, interfaces directly with the IF stages of RF receivers and transmitters using the Model 6236 Dual Channel Wideband Receiver and the Model 6228 Dual Channel Digital Upconverter.

IF signals at 70 MHz with a 10 MHz bandwidth are undersampled using a sampling clock of 60 MHz. The 10 MHz band is translated down to a center frequency of 10 MHz with signals ranging from 5 to 15 MHz. Using a local oscillator setting of 10 MHz, the digital receiver produces a complex (I&Q) output signal with a bandwidth of 10 MHz centered at DC. Baseband data samples from both input channels are delivered across the VIM interfaces to independent Model 4294 G4 PowerPC processing nodes A and B.

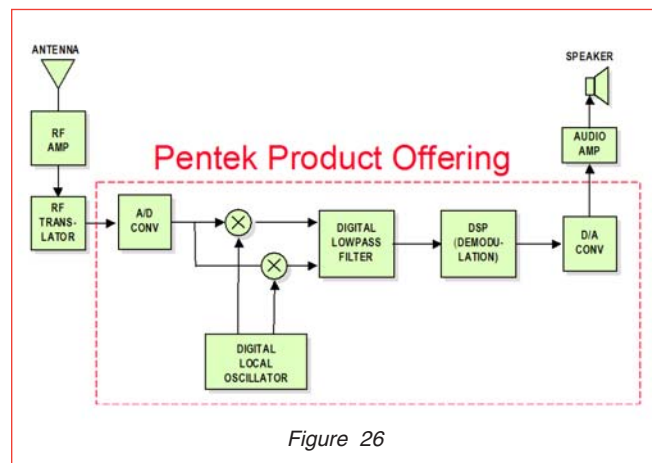
Channel A input baseband signal data (blue) flows from the receiver through processor nodes A and D and out to the Model 6228 Digital Upconverter using the Global PCI Bus. Channel B data (red) flows through processor nodes B and C using the IP PCI Bus. These two completely independent signal paths allow high-bandwidth pipelined processing.

The Model 6228 Upconverter interpolates the output baseband signal up to a sampling rate of 320 MHz and then translates it to a center frequency of 70 MHz. Finally, the samples are delivered to two 320 MHz 16-bit D/A converters producing analog outputs ready for an IF input port. This entire transceiver system occupies a single 6U VMEbus slot!

Two Virtex-II FPGAs, one on the 6236 and one on the 6228 support custom signal processing algorithms for baseband input and output signals.

## Products

### Digital Receiver System Products



As shown in Figure 26, Pentek offers standard off-the-shelf products for everything after the RF translator and up to the D/A converters.

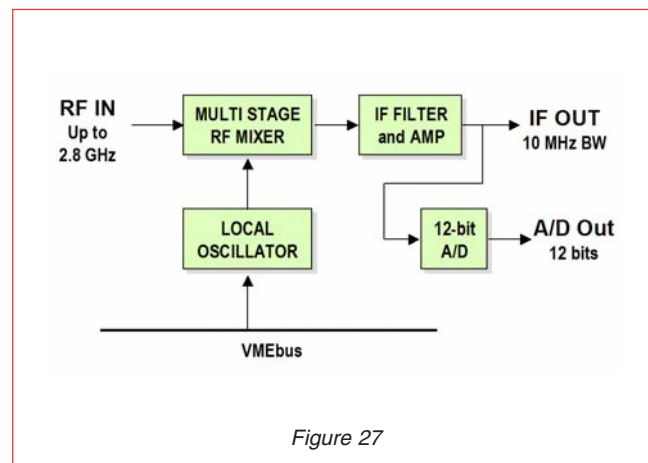
These products are modular, easy-to-use, and flexible enough to provide a virtually unlimited range of system configurations.

Using the block diagram above, we will start with the RF translator function and work through a description of available products from left to right.

All of the many digital receiver products offered by Pentek are completely compatible and are supported by comprehensive suites of software development tools.

As you develop your system, our fully-trained staff of application engineers can guide you through your design and help you get the most out of your system.

### RF Translator



In case the frequency of the RF input signal is too high for direct A/D conversion or for undersampling, an RF receiver or translator must precede the A/D.

These devices, often referred to as “slot receivers,” are implemented using analog RF circuitry including conventional analog mixers, amplifiers and filters. The tuning is usually accomplished by setting the frequency of a local oscillator so that the signal of interest is translated down to an IF frequency, just as in our analog receiver described in the beginning.

A typical RF translator shown in Figure 27, uses the popular IF frequency of 21.4 MHz. Using an IF bandwidth of 10 MHz allows any translated 10 MHz band from DC up to 2.8 GHz to be centered at 21.4 MHz, well within the alias-free sampling range of a 12-bit A/D operating at 65 MHz.

In some designs, an optional A/D converter may be included to simplify system complexity.

Note that the local oscillator only needs to be tuned with relatively coarse steps, say 1 MHz, to ‘ballpark’ the translated signal. All of the fine tuning can be performed by the digital receiver stage which follows. In some dedicated applications, the signal of interest may lie within a very narrow range of frequencies and the local oscillator can be a fixed frequency signal.

These products are available from several vendors.

## Products

### Digital Receiver and FPGA Selection Guide

|              |      |       |       |       | Number of Receiver Channels |            |          |          |          | Number of FPGAs |           |          |           |           |
|--------------|------|-------|-------|-------|-----------------------------|------------|----------|----------|----------|-----------------|-----------|----------|-----------|-----------|
| Pentek Model | Type | Form  | Input | Ouput | TI/CG 4016                  | TI/CG 1012 | Core 421 | Core 422 | Core 430 | XCV 600         | XC2V 3000 | XC2VP 50 | XC2VP 100 | XC4V SX55 |
| 6230         | NB   | VIM-4 | Ana   | VIM   | 32                          |            |          |          |          | 2               |           |          |           |           |
| 6231         | NB   | VIM-2 | Ana   | VIM   | 16                          |            |          |          |          | 1               |           |          |           |           |
| 6232         | NB   | VIM-4 | Dig   | VIM   | 32                          |            |          |          |          | 2               |           |          |           |           |
| 6235         | WB   | VIM-2 | Ana   | VIM   |                             | 2          | 2        |          |          |                 | 1         |          |           |           |
| 6236         | WB   | VIM-2 | Ana   | VIM   |                             | 2          | 2        |          |          |                 | 1         |          |           |           |
| 6250         | MB   | VIM-2 | FPDP  | VIM   |                             |            | 4        | 4        |          |                 | 2         |          |           |           |
| 6251         | MB   | VIM-2 | FPDP  | VIM   |                             |            | 4        | 4        |          |                 |           | 2        |           |           |
| 6821         | MB   | VME   | Ana   | FPDP  |                             |            | 2        | 2        |          |                 |           | 2        |           |           |
| 6822         | MB   | VME   | Ana   | FPDP  |                             |            | 2        | 2        |          |                 |           | 2        |           |           |
| 6823         | MB   | VME   | Ana   | FPDP  |                             |            |          |          |          |                 |           |          |           | 4         |
| 6826         | MB   | VME   | Ana   | FPDP  |                             |            |          |          |          |                 |           |          | 1         |           |
| 7131         | MB   | PMC   | Ana   | PCI   | 16                          |            |          |          |          |                 | 1         |          |           |           |
| 7140         | MB   | PMC   | Ana   | PCI   | 16                          |            |          |          | 256      |                 |           | 1        |           |           |
| 7231         | MB   | cPCI  | Ana   | PCI   | 32                          |            |          |          |          |                 | 2         |          |           |           |
| 7240         | MB   | cPCI  | Ana   | PCI   | 32                          |            |          |          | 512      |                 |           | 2        |           |           |
| 7631         | MB   | PCI   | Ana   | PCI   | 16                          |            |          |          |          |                 | 1         |          |           |           |
| 7640         | MB   | PCI   | Ana   | PCI   | 16                          |            |          |          | 256      |                 |           | 1        |           |           |

NB: Narrowband, WB: Wideband, MB: Multiband, Dig: Digital, Ana: Analog, FPDP: Front Panel Data Port

The above chart shows a model number listing of Pentek digital receiver products showing receiver band type, form factor and input/output characteristics.

The center section shows the number of channels of each type of digital receiver used in each product. The GateFlow IP Cores 421, 422 and 430 shown are available as factory installed options in certain products.

The right section of the chart shows the type and number of FPGAs used in each product. The largest device available is shown at the top of the column but smaller members of the same family are optionally available.

For the latest complete list and full specifications of all digital receiver products be sure to visit online Pentek's Software Radio Central:

[pentek.com/sftradcentral](http://pentek.com/sftradcentral)

For the latest listings and descriptions of Pentek's GateFlow IP be sure to visit FPGA Resources online at:

[pentek.com/gateflow](http://pentek.com/gateflow)

## Products

### 215 MHz, 12-bit A/D and FPGA-based Digital Receiver - VME

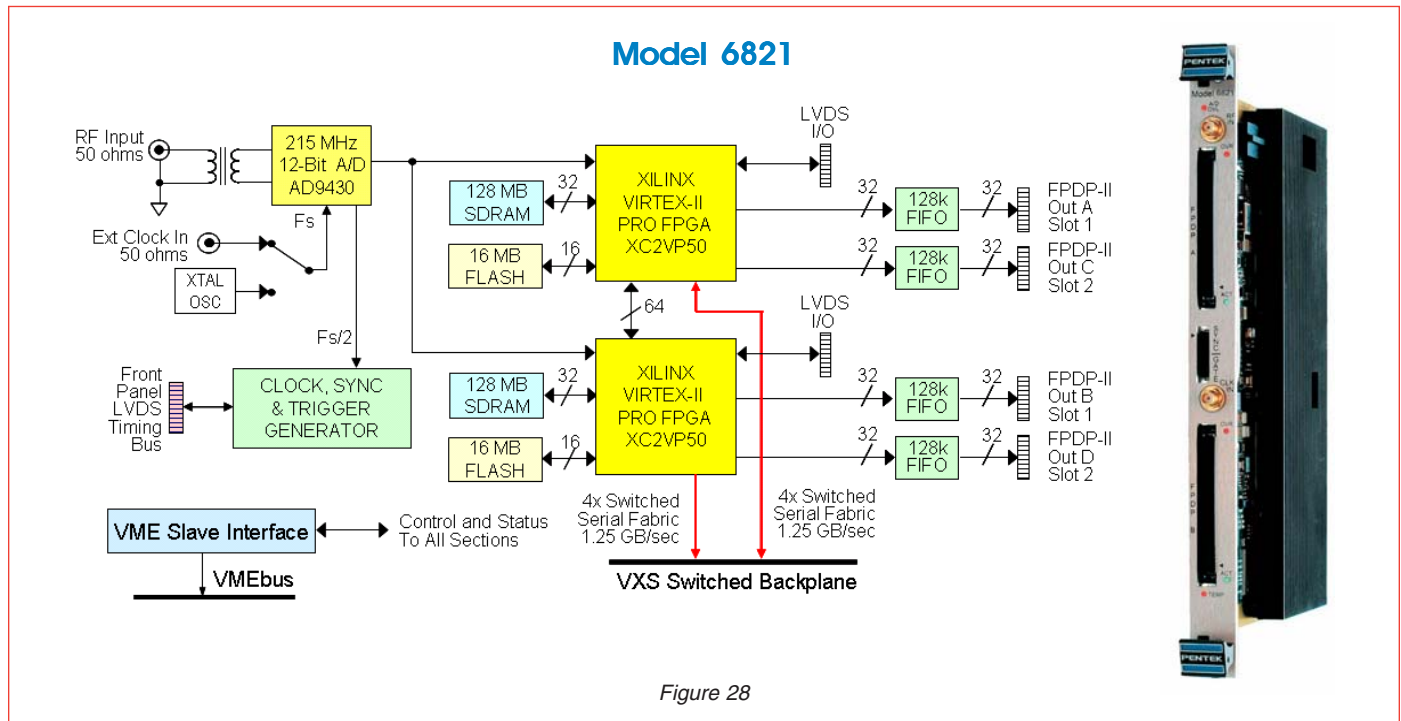


Figure 28

The Model 6821 shown in Figure 28 is a 6U single slot board with the new AD9430 12-bit 215 MHz A/D converter.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from the A/D converter flows into two Xilinx Virtex-II Pro FPGAs where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Because the sampling rate is well beyond conventional ASIC digital downconverters, none are included on the board.

Instead, the Pentek GateFlow IP Core 422 Ultra Wideband Digital Downconverter can be used in one or

both of the FPGAs to perform this function. This core can be incorporated by the customer using the GateFlow FPGA Design Kit or ordered as a factory installed option. Visit [pentek.com/gateflow](http://pentek.com/gateflow) for more information.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

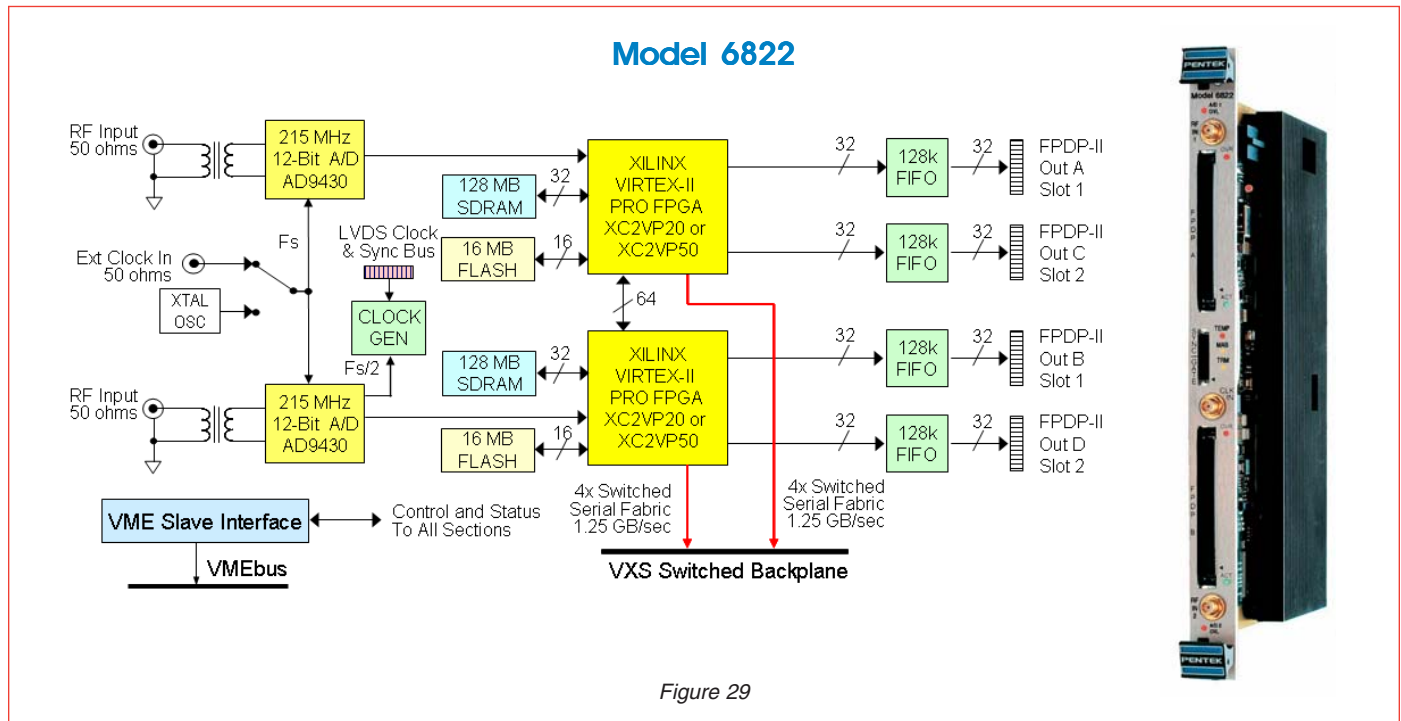
A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

This Model is available in commercial as well as conduction-cooled versions.



## Products

### Dual 215 MHz, 12-bit A/D and FPGA-based Digital Receiver - VME



The Model 6822 shown in Figure 29 is a 6U single slot VME board with two AD9430 12-bit 215 MHz A/D converters.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from each A/D converter flows into a Xilinx Virtex-II Pro FPGA where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Because the sampling rate is well beyond conventional ASIC digital downconverters, none are included on the board.

Instead, the Pentek GateFlow IP Core 422 Ultra Wideband Digital Downconverter can be used in each FPGA to perform this function. This core can be

incorporated by the customer using the GateFlow FPGA Design Kit or ordered as a factory installed option. Visit [pentek.com/gateflow](http://pentek.com/gateflow) for more information.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

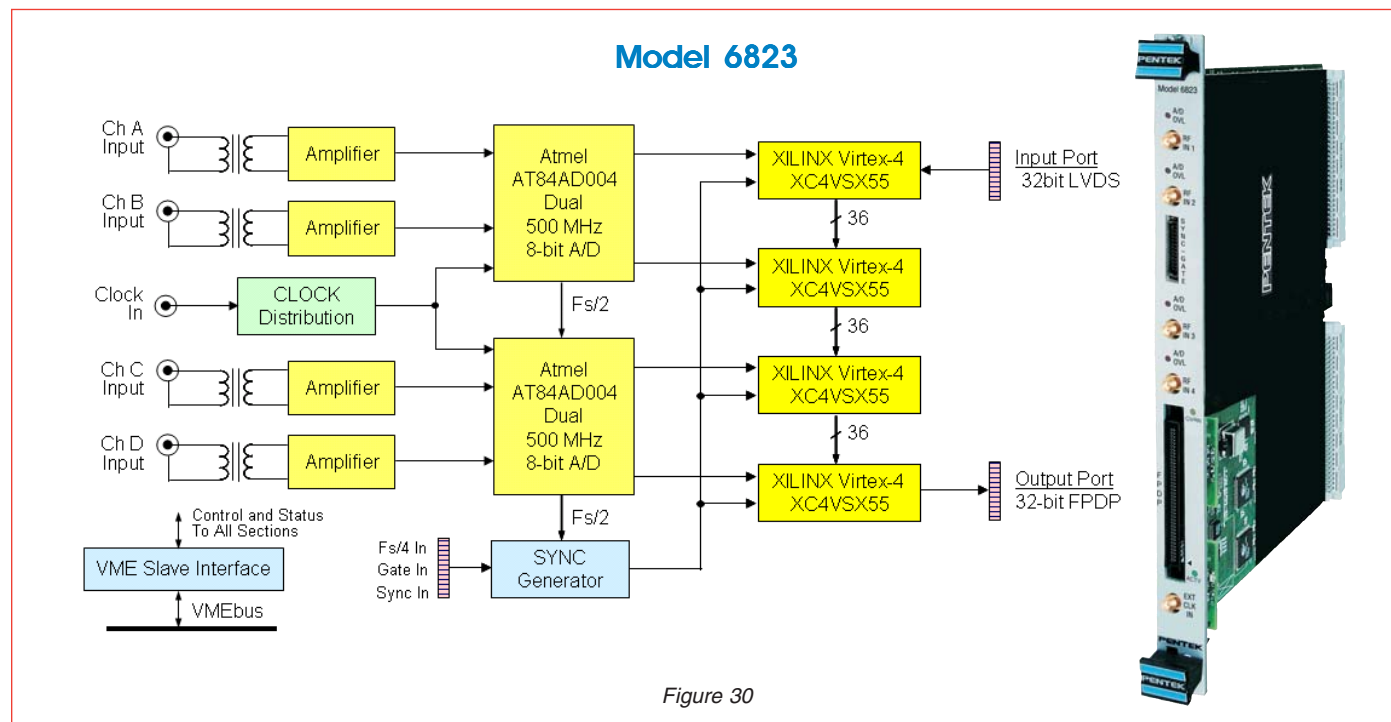
Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

This Model is available in commercial as well as conduction-cooled versions.

## Products

### Quad 500 MHz, 8-bit A/D and FPGA-based Digital Receiver - VME



The Model 6823 shown in Figure 30 is a 6U single slot VME board with two dual Atmel AT84AD004 500 MHz 8-bit A/D converters.

Capable of digitizing input signals at sampling rates up to 500 MHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems. The sampling clock is derived from an external sinusoidal source.

Data from each of the four A/D converters flows into one of four Xilinx Virtex-4 XC4VSX55 FPGAs where optional signal processing functions can be performed. As the largest FPGA in the SX family, the XC4VSX55 is rich in processing resources.

Because the sampling rate is well beyond conventional ASIC digital downconverters, none are included on the board. A very high-speed digital downconverter

IP core for the Model 6823 is currently under development at Pentek.

The customer will be able to incorporate this core into the Model 6823 by using the GateFlow FPGA Design Kit, or order it as a factory installed option.

An input LVDS front panel 32-bit port is connected to the first FPGA of the FPGA chain, while a 32-bit FPDP or FPDP II front panel port connects to the last FPGA for moving data out of the FPGA. Both ports support data transfers of 320 MB/sec and higher.

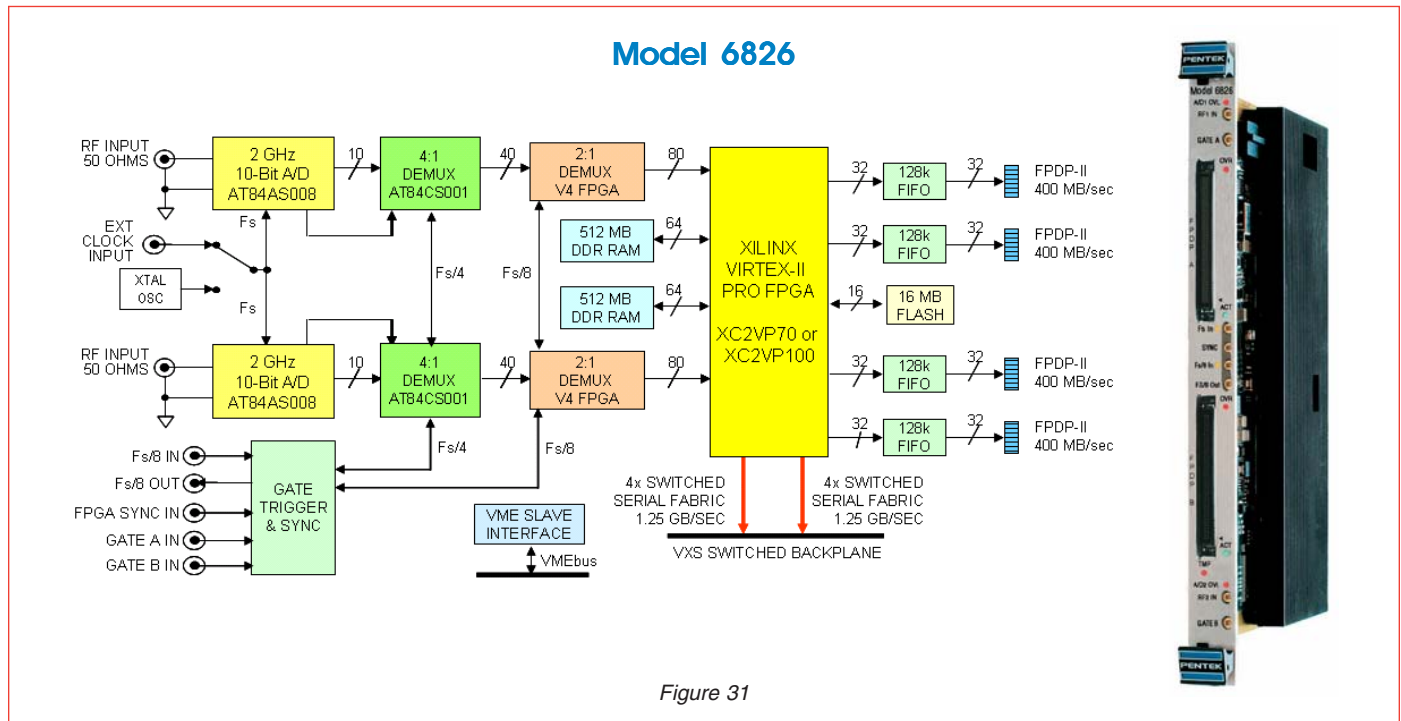
This architecture supports channelized applications such as communication systems and data summation applications such as beamforming.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides control paths for runtime applications.



## Products

### Dual 2 GHz, 10-bit A/D and FPGA-based Digital Receiver - VME



The Model 6826 shown in Figure 31 is a 6U single slot VME board with two Atmel AT84AS008 10-bit 2 GHz A/D converters.

Capable of digitizing input signals at sampling rates up to 2 GHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems. The sampling clock is an externally supplied sinusoidal clock at a frequency from 200 MHz to 2 GHz.

Data from each of the two A/D converters flows into an innovative dual-stage demultiplexer that packs groups of eight data samples into 80-bit words for delivery to the Xilinx Virtex-II Pro XC2VP70 or XC2VP100 FPGA at one eighth the sampling frequency. This advanced circuit features the Atmel AT84CS001 demultiplexer which represents a significant improvement over previous technology.

Because the sampling rate is well beyond conventional ASIC digital downconverters, none are included on the board. A very high-speed digital downconverter

IP core for the Model 6826 is currently under development at Pentek.

The customer will be able to incorporate this core into the Model 6826 by using the GateFlow FPGA Design Kit, or order it as a factory installed option.

Two 512 MB or 1 GB SDRAMs, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

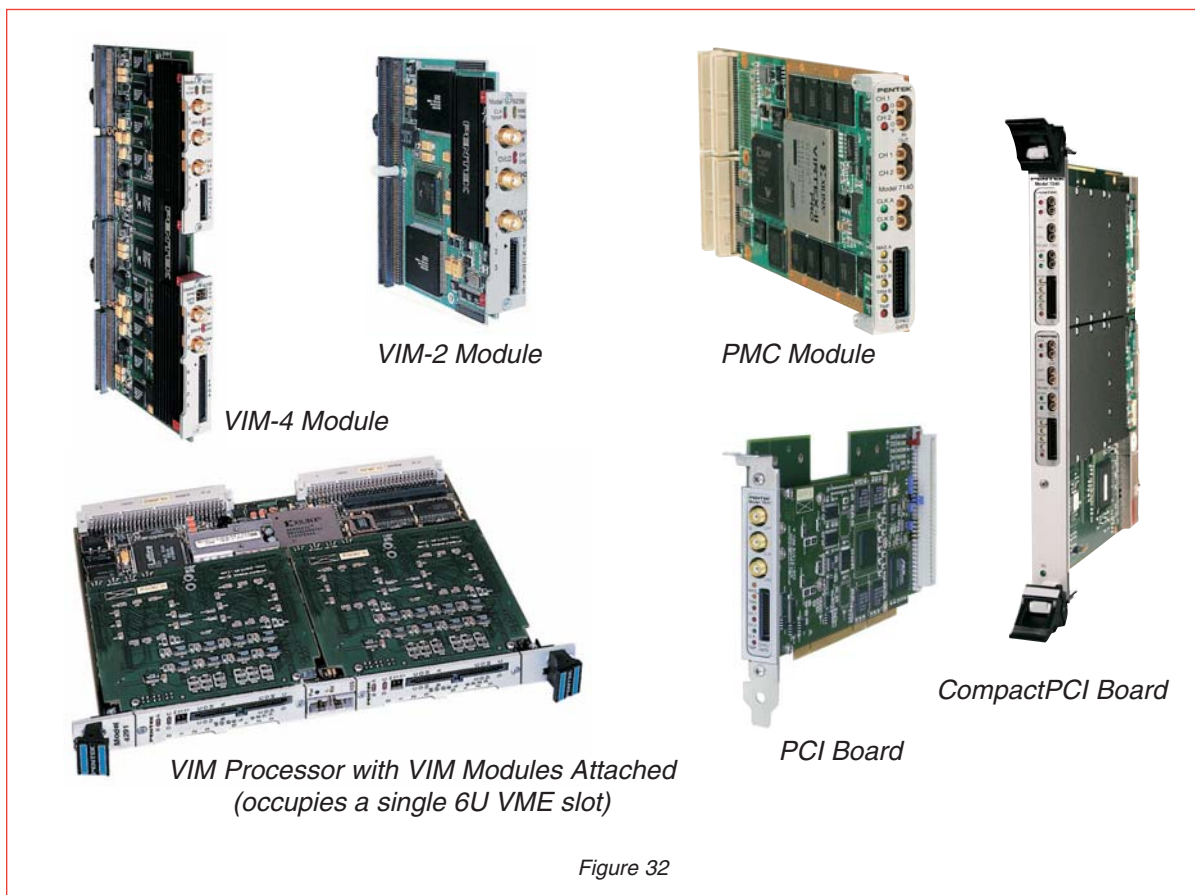
Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

This Model is available as a single-channel version and in commercial as well as conduction-cooled versions.

## Products

### VIM, PMC, PCI and CompactPCI Digital Receivers



Pentek's latest family of processor and software radio products take advantage of a new architecture called VIM, for Velocity Interface Mezzanine.

VIM provides a direct path between daughter or mezzanine cards and quad VMEbus processor boards so that each processor has its own private, dedicated channel for high-speed digital data at rates up to 400 MB/sec. With four of these interfaces on each quad processor board the total mezzanine I/O peak bandwidth is an impressive 1600 MB/sec.

Pentek offers several VIM processor boards based on the Texas Instruments DSP chips TMS320C6201, C6701 and the C6203; and the Freescale AltiVec G4 PowerPC.

VIM mezzanine modules attach to these processor boards and nest in the same slot providing very high

density single-slot subsystems. The front panels of the VIM modules actually replace sections of the front panel of the processor boards.

VIM modules are available in two formats: the VIM-2 that connects to two processors and the VIM-4 which connects to four. By attaching two different types of VIM-2 modules, you can create unique combinations of software radio functions and high-speed interfaces.

For an overview of VIM and a complete listing of VIM-compatible products, visit VIM Central on our website at [pentek.com/vimcentral](http://pentek.com/vimcentral).

Pentek also offers products in three form factors for PCI bus: PMC (PCI Mezzanine Card) modules, PCI boards and CompactPCI boards.

## Products

### 32-Channel Narrowband Digital Receiver with A/D and FPGA - VIM-4

Model 6230

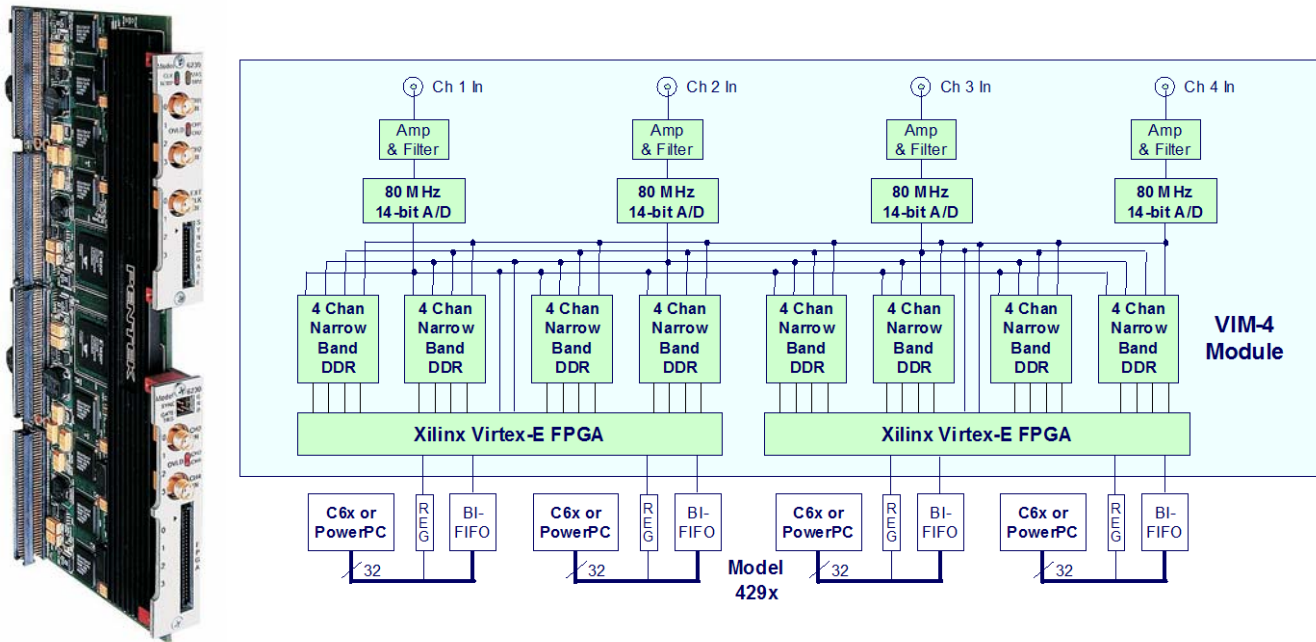


Figure 33

The Model 6230 is a feature-packed VIM-4 module that includes four A/D converters, 32 narrowband digital receiver channels and two FPGAs. Coupled with a VIM processor board, the Model 6230 creates an extremely powerful receiver system at a very low cost per channel. It exemplifies the “channelized” system concept, with each segment of the signal processing chain in a single VMEbus slot. Also available is the Model 6231, the VIM-2 version, with two A/Ds, 16 narrowband channels, and one FPGA.

Four front panel SMA connectors accept RF analog inputs which are conditioned by an input amplifier and a bypassable low pass anti-aliasing filter. These inputs are digitized by four AD6645 14-bit 80 MHz A/D converters. The sampling clock is derived from an internal 80 MHz crystal oscillator, an external front panel reference input, or from an LVDS front panel ribbon cable clock and sync board that can be used to synchronize multiple 6230s.

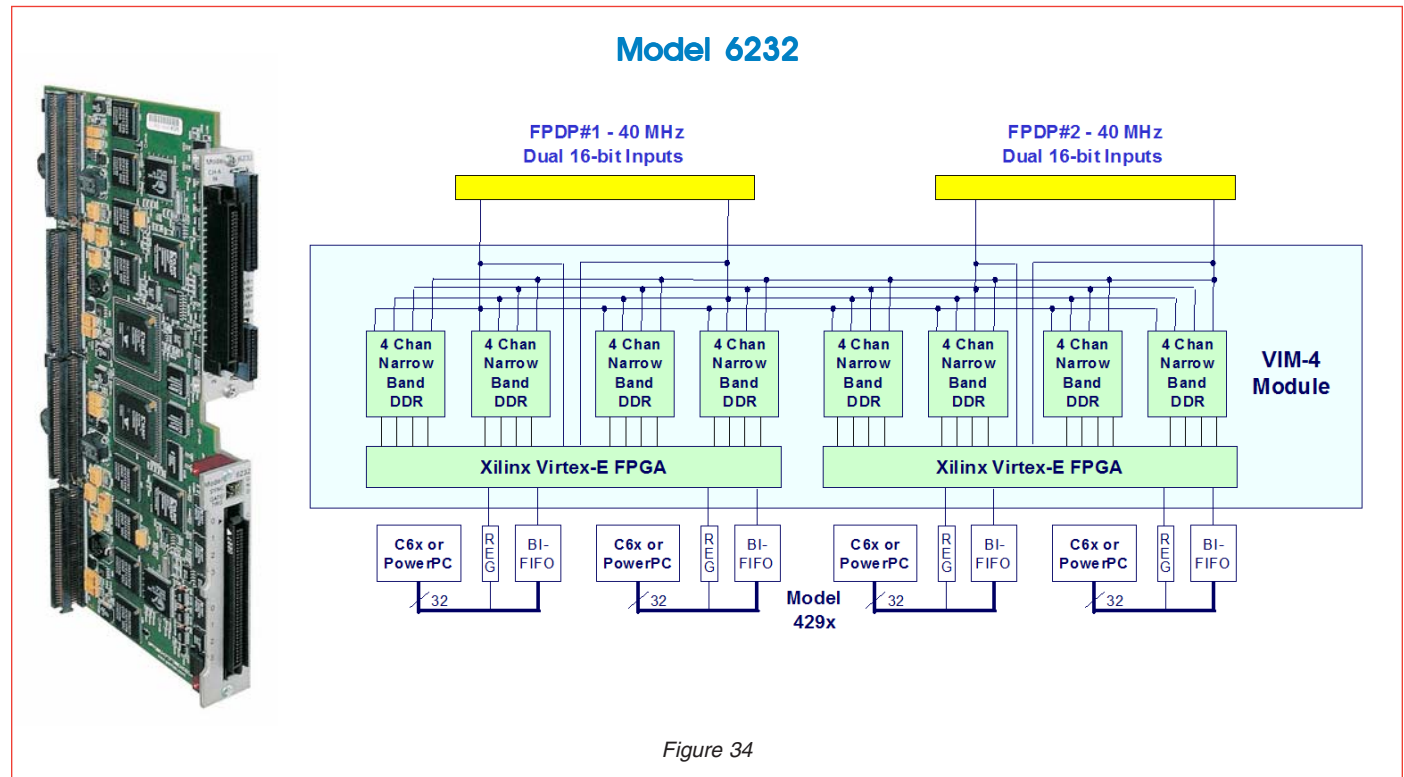
All four A/D digital outputs are delivered to eight GC4016 quad narrowband digital receivers, so that each receiver channel can independently select its source from any one of the four A/D converters. Each receiver channel can be independently tuned and custom filter coefficients can be downloaded to each channel’s FIR filter.

The narrowband receiver outputs and the wideband A/D outputs are delivered into two Xilinx Virtex-E FPGAs with 300k or 600k gate densities (XCV300 or 600). Factory default features programmed into the FPGA include the VIM interface, digital receiver bypass (direct A/D into the VIM interface) mode, narrowband channel selection, and various packing modes. An optional FPGA development kit allows custom algorithms to be implemented.

Other front panel features include a connector for 32 FPGA user I/O lines, two TTL inputs for triggering and gating, and RF input overload detectors.

## Products

### 32-Channel Narrowband Digital Receiver with FPDP and FPGA - VIM-4



The Model 6232 is the digital input counterpart of the Model 6230. Instead of four A/D converters, the Model 6232 features two FPDP (Front Panel Data Port) input connectors. FPDP is an industry standard interconnection scheme for transferring 32-bit digital data between two devices using flat ribbon cable. Clock rates up to 40 MHz are supported. FPDP II, the second generation of FPDP, achieves rates up to 100 MHz.

Each 32-bit FPDP port is divided into two 16-bit fields so that two digitized input signals can be brought in over each port at sampling rates up to 40 MHz.

All four 16-bit digital input words are connected to the inputs of eight GC4016 quad narrowband digital receivers, so that each receiver channel can independently select its source from any one of the four A/D converters. Like the 6230, each receiver channel can be independently

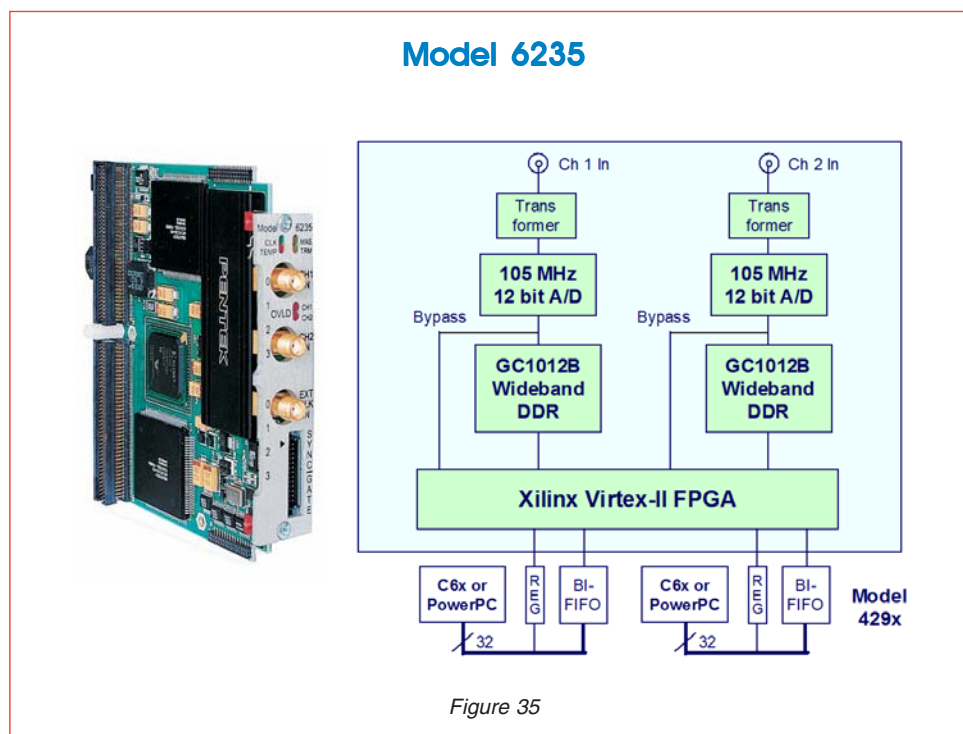
tuned and custom filter coefficients can be downloaded to each channel's FIR filter.

Again, using an architecture similar to the Model 6230, the narrowband receiver outputs and the wide-band FPDP digital inputs are delivered into two Xilinx Virtex-E FPGAs in sizes ranging from 300k to 600k gate densities. Again, factory default features of the FPGA include the VIM interface, digital receiver bypass (direct FPDP data into the VIM interface) modes, narrowband channel selection, and various packing modes. An optional FPGA development kit allows custom algorithms to be implemented.

Other features include two clock deskewing FIFO's at the FPDP inputs to realign data coming from two sources with variable delay characteristics.

## Products

### Dual Channel A/D and Wideband Receiver with FPGA - VIM-2



The Model 6235 Dual Channel Wideband Receiver in Figure 35 is primarily intended for digitizing wideband IF input signals. Each RF input is transformer-coupled to the A/D converter to support input signals up to 150 MHz for undersampling applications.

Two AD9432 A/D converters digitize the RF inputs to 12-bit samples. The sampling clock is derived from an internal 100 MHz crystal oscillator, an external front panel reference input or from an LVDS front panel ribbon cable clock and sync board that can be used to synchronize multiple 6235s. As many as 80 Model 6235's can be synchronized with Pentek's Model 9190 Clock and Sync Generator to support systems with many channels.

The A/D digital outputs feed two TI/Graychip GC1012B wideband receivers, capable of accepting data at the 100 MHz rate. These chips can be set for decimation values to support output bandwidths from 1.25 MHz to 40 MHz.

Both A/D outputs and both wideband receiver outputs are delivered into a Xilinx Virtex-II Series FPGA. Here, factory default logic allows channel selection, triggering, receiver bypass, and data packing modes.

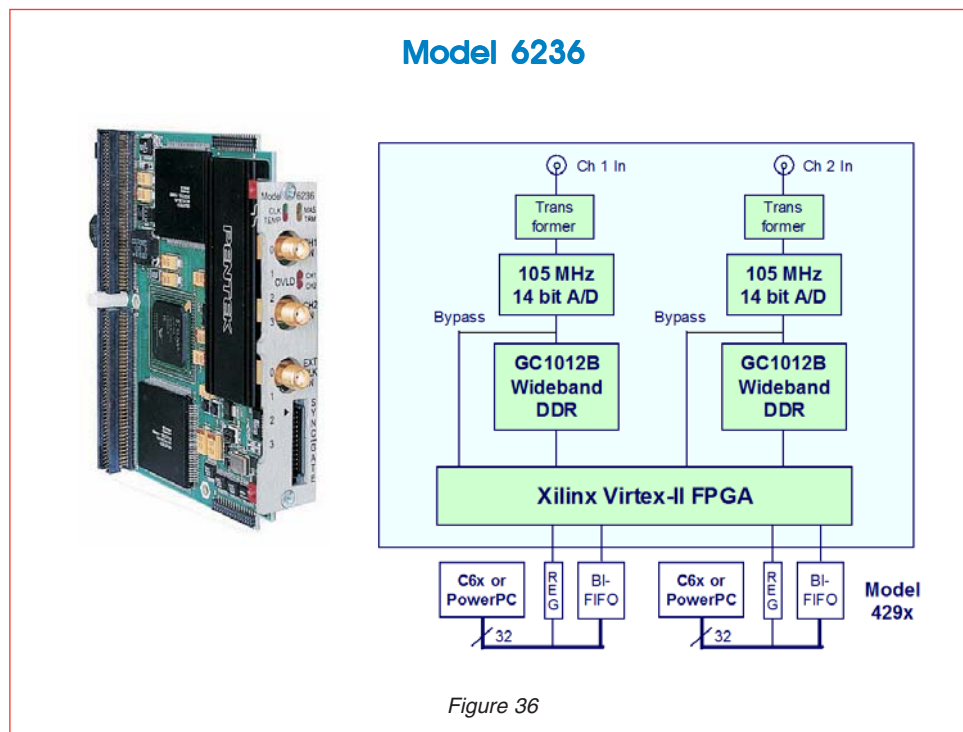
FPGA densities range from 1 to 3 million gates (XC2V1000 or 3000) and an optional GateFlow FPGA Design Kit is available to support user-defined custom algorithms.

See the Model 6236 on the next page for GateFlow FPGA IP Core options also available on the 6235.



## Products

### Dual Channel A/D and Wideband Receiver with FPGA - VIM-2



The Model 6236 is identical to the popular 6235 but incorporates two new 105 MHz 14-bit A/D Converters (Analog Devices AD6645-105). These converters offer two additional bits of resolution for improved accuracy and dynamic range over the 6235.

In addition to the GateFlow FPGA Design Kit, Pentek offers several popular GateFlow IP Cores as factory installed options for both the Model 6235 and Model 6236.

For applications requiring FFTs, two different installed FFT cores are available for either 1k- or 4k-point block sizes (Cores 401 and 404). A complete radar pulse compression core has also been developed specially for the 6235 and 6236 (Core 440).

Because the TI/GC1012B wideband digital receivers accept only 12-bit inputs, two of the A/D converter bits remain unused.

To take advantage of the additional A/D resolution, Pentek's GateFlow Wideband Digital Receiver IP Core 421 can be factory installed in the FPGA, supporting a full 16-bit input, improved dynamic range, and user-configurable FIR filter coefficients. For this reason, the GC1012B chips are offered as an option to save cost.

See page 10 for more information on factory installed IP Cores and visit the GateFlow Resources website for all the latest information: [pentek.com/gateflow](http://pentek.com/gateflow).

## Products

### Multiband Digital Receivers with A/Ds and FPGAs

**Model 7131 PMC • Model 7631 PCI • Model 7231 6U cPCI • Model 7331 3U cPCI**

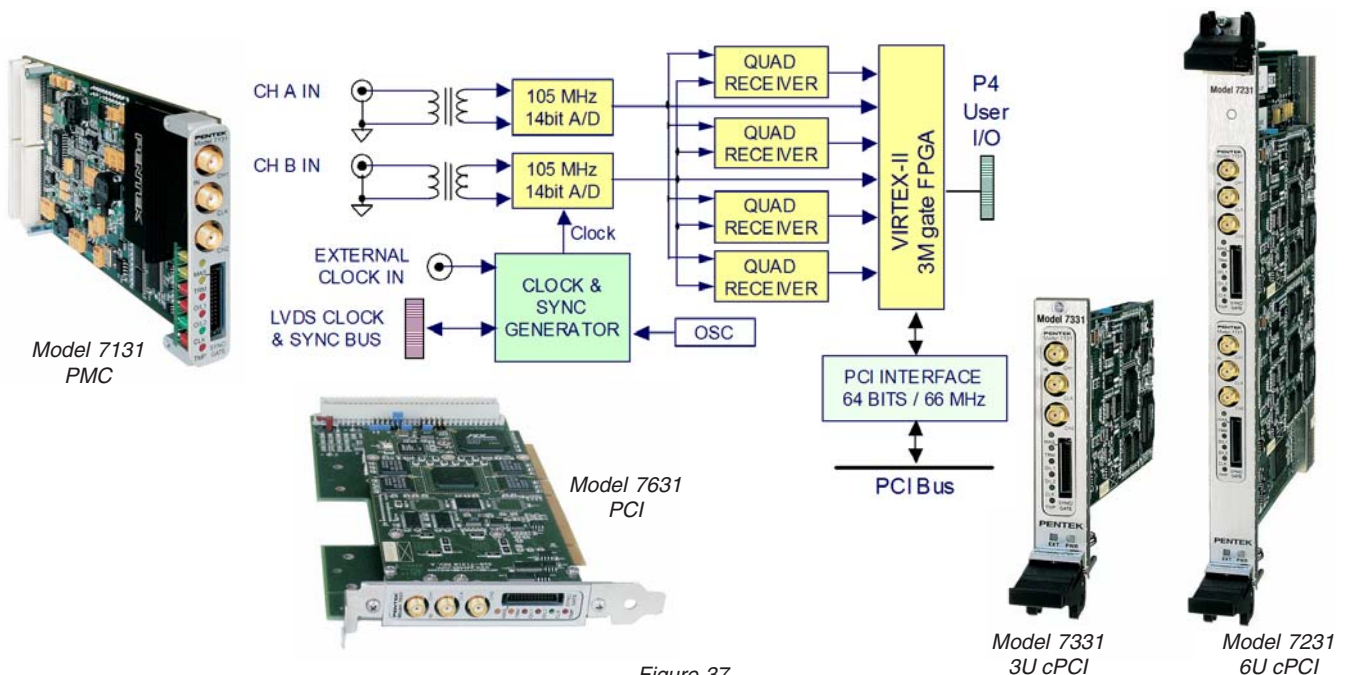


Figure 37

The Model 7131, a 16-Channel Multiband Receiver, is a PMC module. The 7131 PMC may be attached to a wide range of industry processor platforms equipped with PMC sites. The faceplate of a PMC module fits in a cutout on the front panel of the processor board and the PCI bus interface to the processor board is made through connectors at the rear of the module.

Versions of the 7131 are also available as PCI boards (7631) and 6U or 3U CompactPCI boards (7231 or 7331). All three products have similar features.

Two 14-bit 105 MHz A/D Converters (Analog Devices AD6645) accept transformer-coupled RF inputs through two front panel SMA connectors. Both inputs are connected to four TI/GC4016 quad digital receiver chips, so that all 16 receiver channels can independently select either A/D.

Four parallel outputs from the four receivers deliver data into the Virtex-II FPGA which can be either the XC2V1000 or XC2V3000. The outputs of the two A/D converters are also connected directly to the FPGA to

support the receiver bypass path to the PCI bus and for direct processing of the wideband A/D signals by the FPGA.

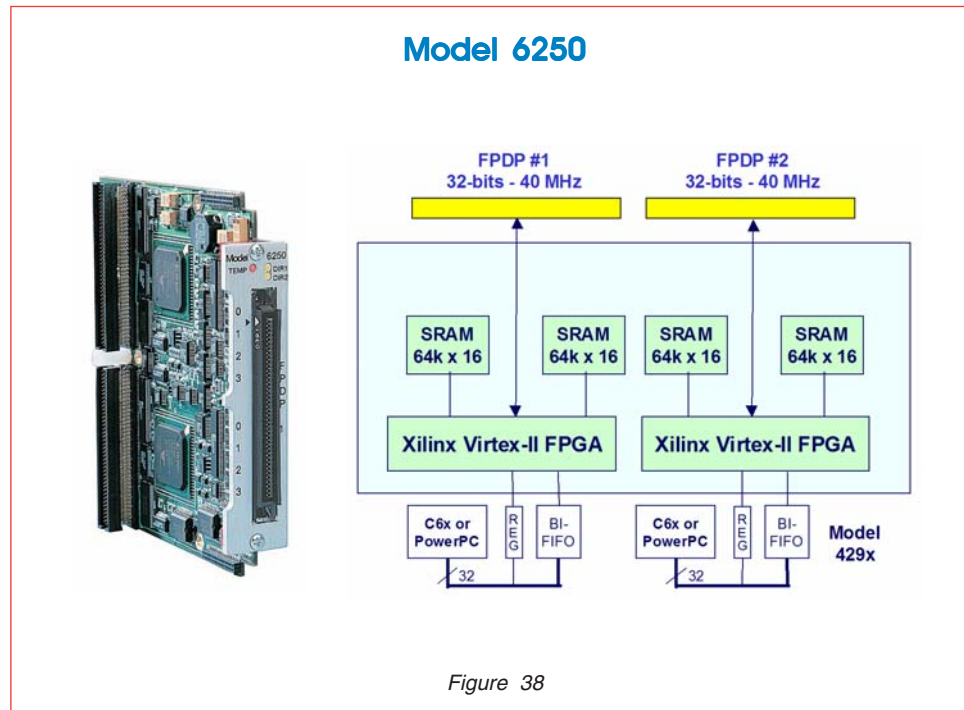
The unit supports the channel combining mode of the 4016s such that two or four individual 2.5 MHz channels can be combined for output bandwidths of 5 MHz or 10 MHz, respectively.

The sampling clock can be sourced from an internal 100 MHz crystal oscillator or from an external clock supplied through an SMA connector or the LVDS clock/sync bus on the front panel. The LVDS bus allows multiple modules to be synchronized with the same sample clock, gating, triggering and frequency switching signals. Up to 80 modules can be synchronized with the Model 9190 Clock and Sync Generator. Custom interfaces can be implemented by using the 64 user-defined FPGA I/O pins on the P4 connector.

The FPGA is fully supported with the GateFlow FPGA Design Kit and GateFlow FPGA IP Core Library. Software drivers support VxWorks, Windows and Linux processor board operating systems.

## Products

### Dual FPDP Adapter with Virtex-II FPGAs - VIM-2



While not actually containing a digital receiver, the Model 6250 Dual FPDP Adapter in Figure 38 supports very high-performance custom signal processing functions by incorporating two high-density FPGAs.

Two bidirectional FPDP ports transfer 32-bit data at clock rates up to 40 MHz. Support for FPDP-II ports allows clock rates as high as 100 MHz (400 MB/sec.)

The FPDP inputs are connected to two Xilinx Virtex-II FPGAs with densities of either 1 or 3 million gates each (XC2V1000 or 3000). The FPGAs are clocked from an on-board 100 MHz crystal oscillator. Factory default FPGA configuration code includes the FPDP interface and the VIM interface so standard units can be used as fast FPDP adapters.

Custom FPGA configuration code can be developed using the optional GateFlow FPGA Design Kit containing the VHDL source for the factory default configuration and provisions for adding user-defined algorithms.

Each FPGA is equipped with two 64k x 16 SRAMs for storing data or coefficients, creating a more powerful environment for custom FPGA applications and incorporation of third party IP cores.

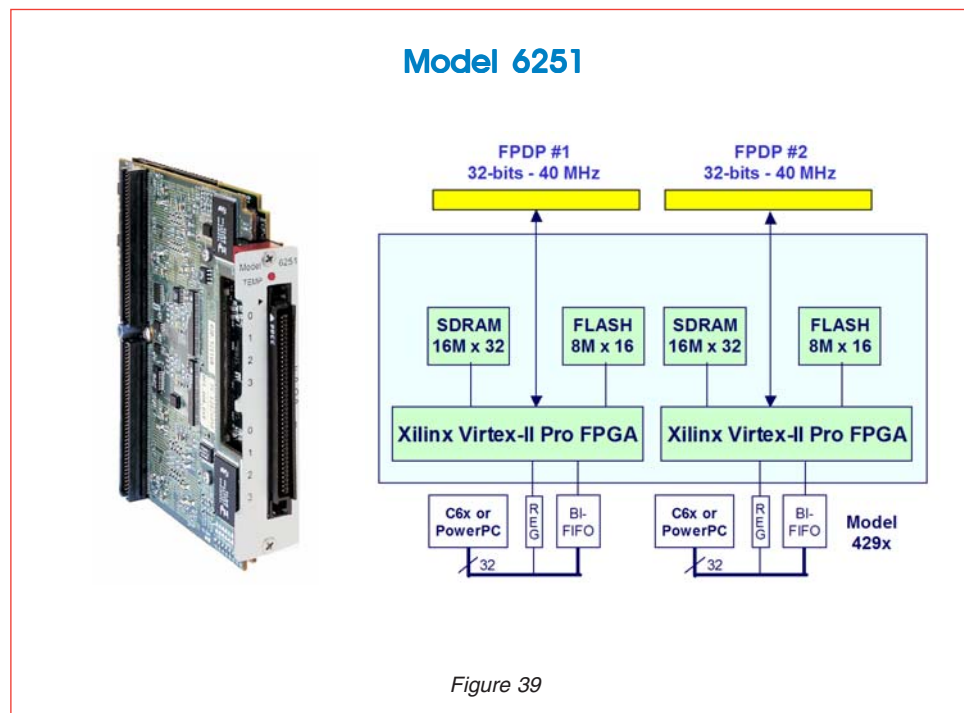
Pentek's GateFlow IP Core Library includes real-time FFTs, wideband digital receivers and pulse compressors which can be used with the GateFlow Design Kit or ordered as factory installed options. Visit Pentek's GateFlow Resources website for the latest information at [pentek.com/gateflow](http://pentek.com/gateflow).

Pentek's family of 68xx A/D converters deliver sampling rates from 215 MHz to 2 GHz and feature FPDP outputs completely compatible with the Model 6250. Since the 6250 can also transmit FPDP data, it can be connected to many other Pentek products including digital receivers, A/Ds and DSP boards.



## Products

### Dual FPDP Adapter with Virtex-II Pro FPGAs and SDRAM - VIM-2



The Model 6251 is the next generation successor to the popular 6250 shown on the previous page.

Major new features of 6251 are two Virtex-II Pro FPGAs that replace the Virtex-II devices with twice the resources plus two embedded PowerPC microcontrollers.

In addition, the four 128 kB SRAMs on the 6250 have been replaced with 64 MByte SDRAMs on the 6251, increasing the memory capacity of the module by a factor of 256.

These larger memories can now support long digital delay lines and large data buffers for transient capture applications. The 16 MB FLASH memories can be used for coefficient or boot code storage for the embedded microcontrollers.

The FPGA sizes range from the XC2VP20 to the XC2VP50 to handle a wide range of applications.

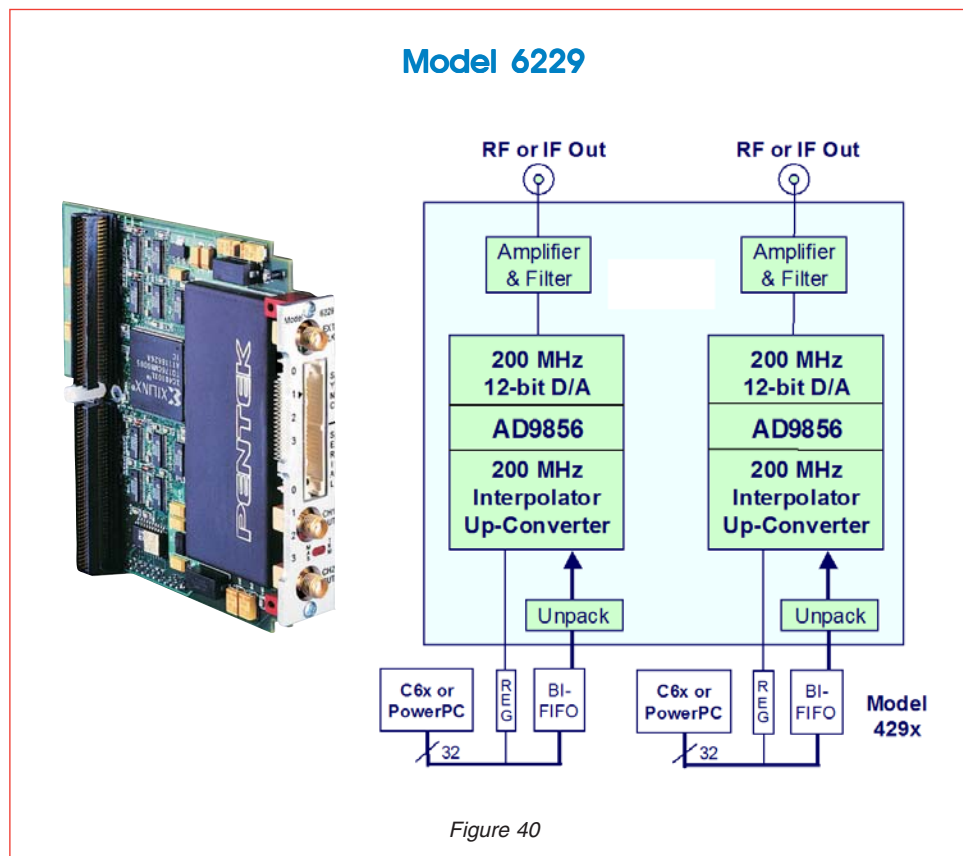
A GateFlow FPGA Design Kit is available for custom algorithm development. It includes all the VHDL source code for the standard factory functions and library functions to support the SDRAM memory.

When used in conjunction with FPDP data sources like Pentek's Series 68xx A/D Converters, the 6251 offers significant signal processing horsepower.

Pentek's GateFlow Wideband Digital Receiver IP Cores 421 and 422 can be used to provide high-speed and high-dynamic range digital downconversion. GateFlow FFT IP Cores 401 and 404 deliver world-class, real-time time-to-frequency domain conversion. The GateFlow Pulse Compression IP Core 440 handles real-time radar pulse compression with block-floating point precision. Visit the GateFlow Resources website at [pentek.com/gateflow](http://pentek.com/gateflow).

## Products

### Dual Channel Wideband Digital Upconverter and D/A - VIM-2



The Model 6229 Dual Channel Wideband Digital Upconverter in Figure 40 complements the digital receiver products by offering an analogous transmit side function.

The Model 6229 employs two AD9856 digital upconverters containing several stages of signal processing within a single monolithic device. The VIM-2 processor delivers complex (I & Q) digital baseband signals at data rates from audio up to 25 Msamples/sec.

The AD9856 uses an interpolation filter to upsample these inputs to a sampling rate of 200 MHz. The signals are then translated in frequency using quadrature mixers with programmable local oscillators.

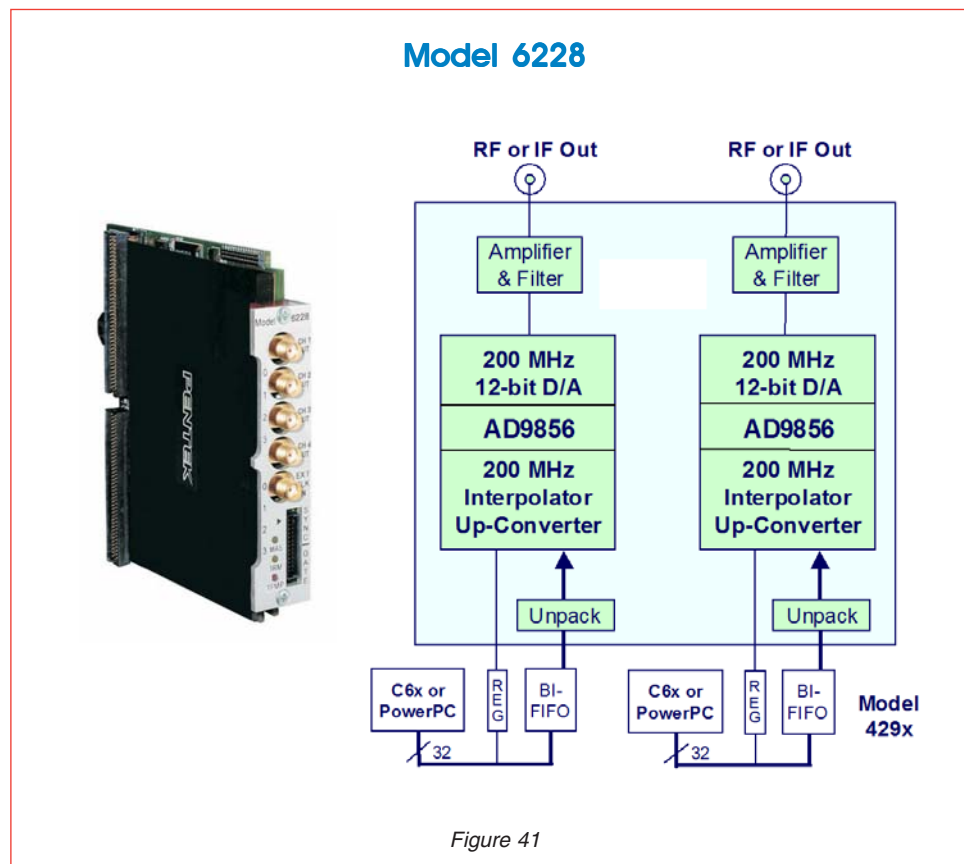
This single-sideband frequency translation allows the baseband signal to be placed anywhere between DC and 80 MHz, suitable for many IF inputs for transmitters or exciters.

Finally, the translated signals are converted to analog by 12-bit 200 MHz D/A converters and delivered to front panel SMA connectors through the output amplifier stages.

The Model 6229 is ideal for developers of new wireless standards, for testing receiver systems and as a general purpose arbitrary waveform generator. The local oscillator can also be used as a CW sinewave oscillator with outputs programmable from DC to 80 MHz.

## Products

### Dual Channel Wideband Digital Upconverter and D/A - VIM-2



The Model 6228 Dual Channel Wideband Digital Upconverter in Figure 41 is the next generation version of the Model 6229.

It uses two Texas Instruments DAC5686 digital upconverter chips that include an interpolation filter, a local oscillator, a complex mixer and two 16-bit D/A converters.

When operated as a digital upconverter, the maximum clock rate is 320 MHz. This allows digital base-band complex input sampling rates up to 80 MHz and output IF frequencies tunable up to 160 MHz.

For the real IF output mode, only one of the 16-bit D/A converters of each DAC5686 is used. For the complex output mode, both D/A converters are used to deliver both I and Q analog signals.

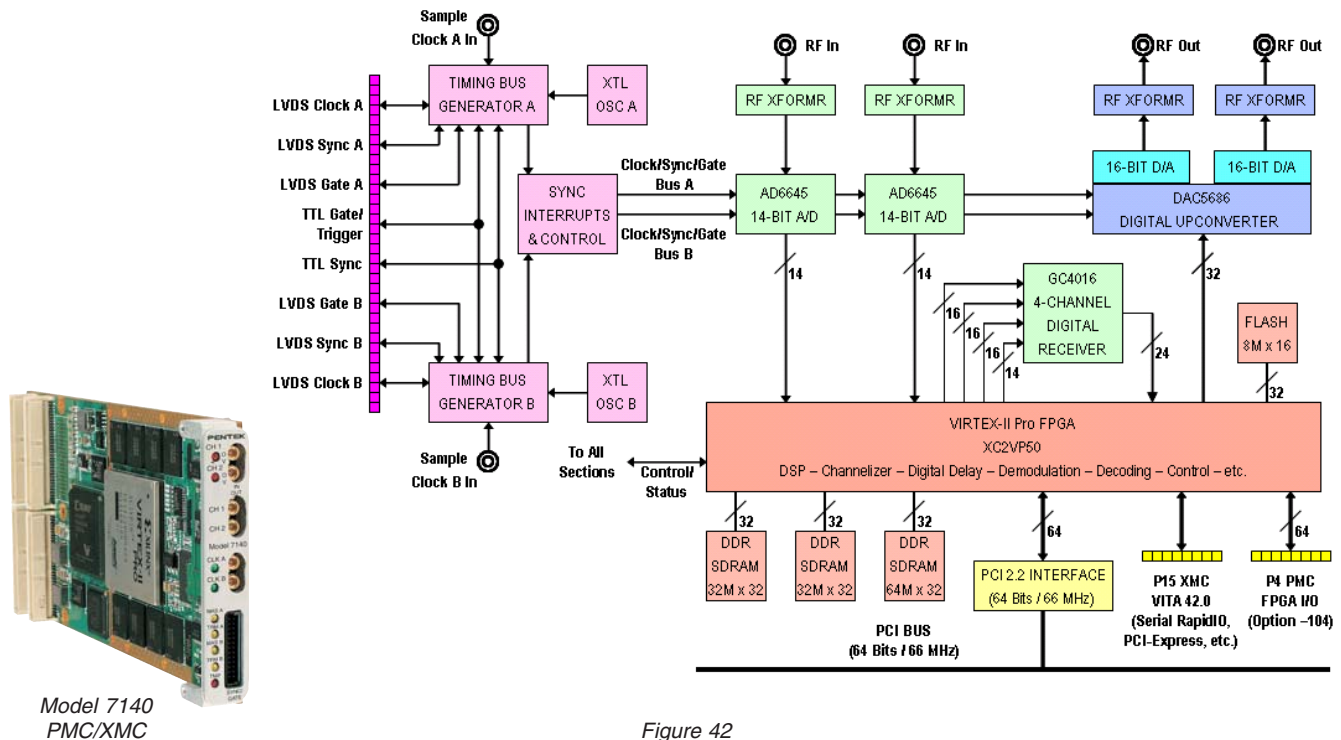
When operated in the D/A only mode, the frequency translation functions are not used. In this mode, the maximum clock frequency for the interpolation filter and D/A converters becomes 500 MHz. With two upconverter chips in the module, four independent data streams can be delivered to the four 16-bit D/A converters, with optional interpolation for generation of signal bandwidths as high as 200 MHz.

The Virtex-II FPGA can be used as a preprocessor front end for the upconverters to implement additional interpolation filtering or other custom signal processing functions. An arbitrary waveform generator could be constructed using internal FPGA memory for waveform storage. A complete GateFlow FPGA Design Kit is available.

## Products

### Digital Upconverters / Downconverters

**Model 7140 PMC/XMC • Model 7640 PCI • Model 7240 6U cPCI • Model 7340 3U cPCI**



The Model 7140 PMC module combines both transmit and receive capability with a high-performance Virtex II-Pro FPGA and supports the emerging VITA 42 XMC standard with optional switched fabric interfaces for high-speed I/O.

The front end of the module accepts two +4 dBm full-scale analog RF inputs and transformer couples them into two 14-bit A/D converters running at 105 MHz. The digitized output signals pass to a Virtex-II Pro FPGA for signal processing or routing to other module resources.

These resources include a quad digital downconverter, a digital upconverter with dual D/A converters, 512 MB DDR SDRAM delay memory and the PCI bus. The FPGA also serves as a control and status engine with data and programming interfaces to

each of the on-board resources. Factory-installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control.

Because the FPGA controls the data flow within the module as well as providing signal processing, the module can be configured for many different functions. In addition to acting as a simple transceiver, the module can perform user-defined DSP functions on the base-band signals, developed using Pentek's GateFlow and ReadyFlow® development tools.

The module includes a TI/GC4016 quad digital downconverter along with a TI DAC5686 digital upconverter with dual D/A converters.

Each channel in the downconverter can be set with an independent tuning frequency and bandwidth. ➤

## Products

### Digital Upconverters / Downconverters

**Model 7140 PMC/XMC • Model 7640 PCI • Model 7240 6U cPCI • Model 7340 3U cPCI**

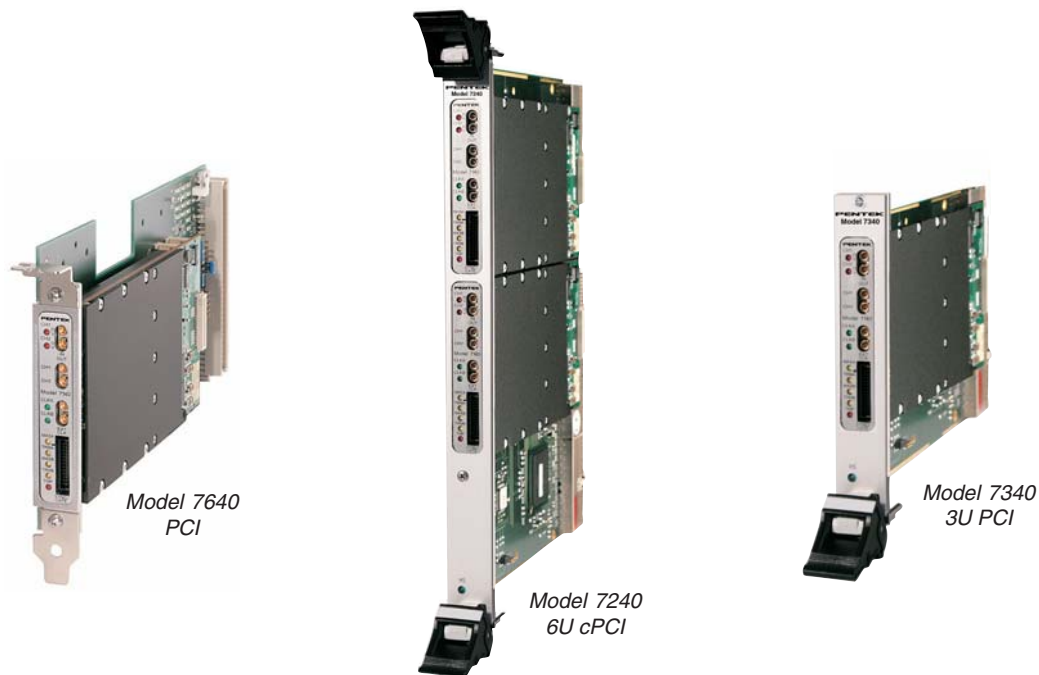


Figure 43

► The upconverter translates a real or complex baseband signal to any IF center frequency from DC to 160 MHz and can deliver real or complex (I + Q) analog outputs through its two 16-bit D/A converters. The digital upconverter can be bypassed for two interpolated D/A outputs with sampling rates to 500 MHz.

Inputs to the downconverter can come from many sources, including the input A/D converters, the FPGA signal processing engines, the SDRAM delay memory, or data sources on the PCI bus. The built-in clock/sync bus supports multiple module synchronization as well as dual on-board oscillators for independent input and output clock rates. Furthermore, the Model 7140 offers the VITA 42 XMC interface. This allows it to transfer data through optional Serial RapidIO, PCI-Express, or other switched fabric interfaces, which provide a high-speed streaming data path that is independent of the PCI bus.

A clock/sync bus allows synchronization of local oscillator phase, frequency switching, decimating filter phase and data collection among multiple 7140s. One board acts as a master, driving clock, sync and gate signals out to a front panel flat cable bus using LVDS differential signaling. The master alone can drive as many as seven slaves. By using a Pentek Model 9190 Clock and Sync Generator to drive the signals, as many as 80 modules can be configured to operate synchronously.

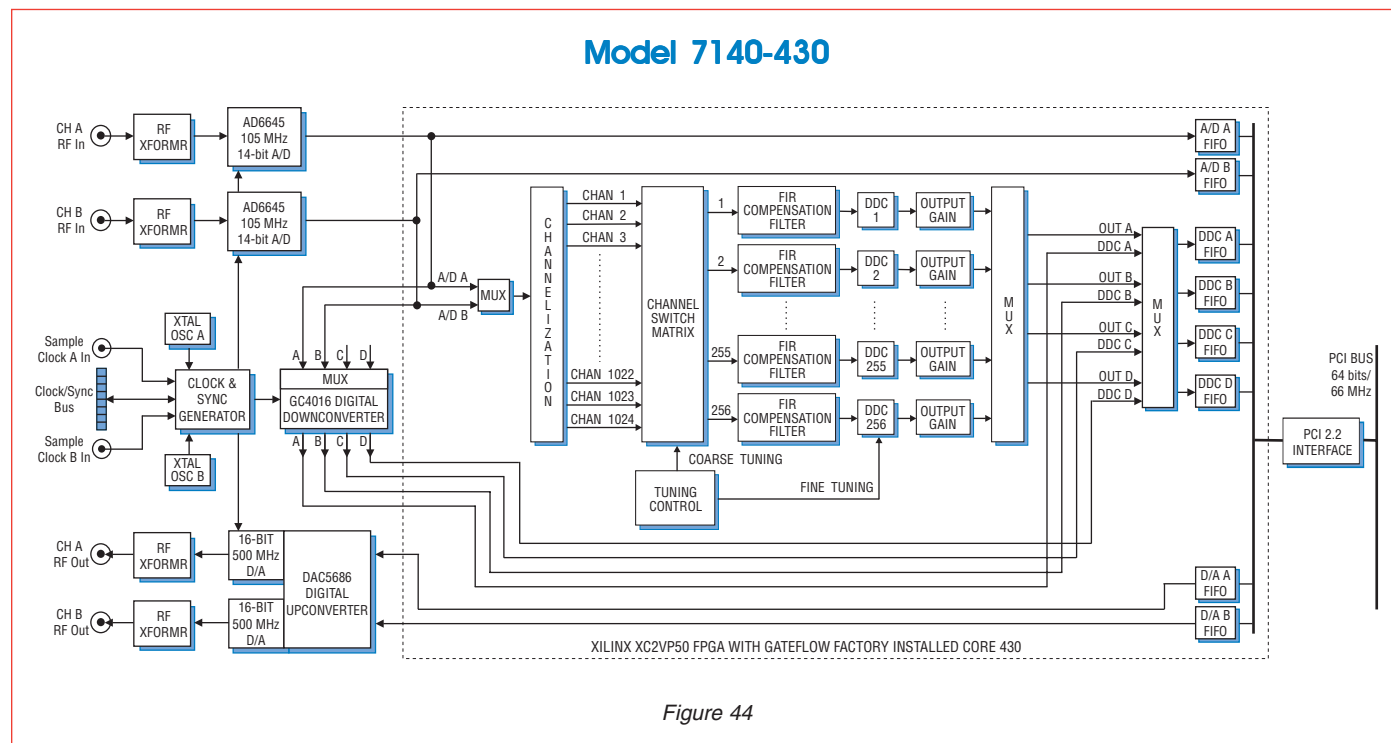
For more information on the Model 7140 Software Radio Transceiver, visit [pentek.com/sftradcentral](http://pentek.com/sftradcentral).

As shown in Figure 43, this module is also available in a variety of form factors including PCI (Model 7640), 3U cPCI (Model 7340), 6U cPCI (Model 7240 with twice the density of the other models) and a PMC conduction-cooled version (Model 7140-700). These models are also available with IP Core 430, a 256-channel narrowband receiver, installed, see the next page for more information.



## Products

### Transceiver with 256-Channel Narrowband DDC Installed Core



For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-channel digital downconverter bank. Factory installed in the Model 7140 FPGA as shown in Figure 44, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

Unlike classic channelizer methods, the Pentek 430 core allows for completely independent programmable tuning of each individual channel with 32-bit resolution as well as filter characteristics comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 8192 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC filter coefficient sets are included with the core for all possible decimation settings.

Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

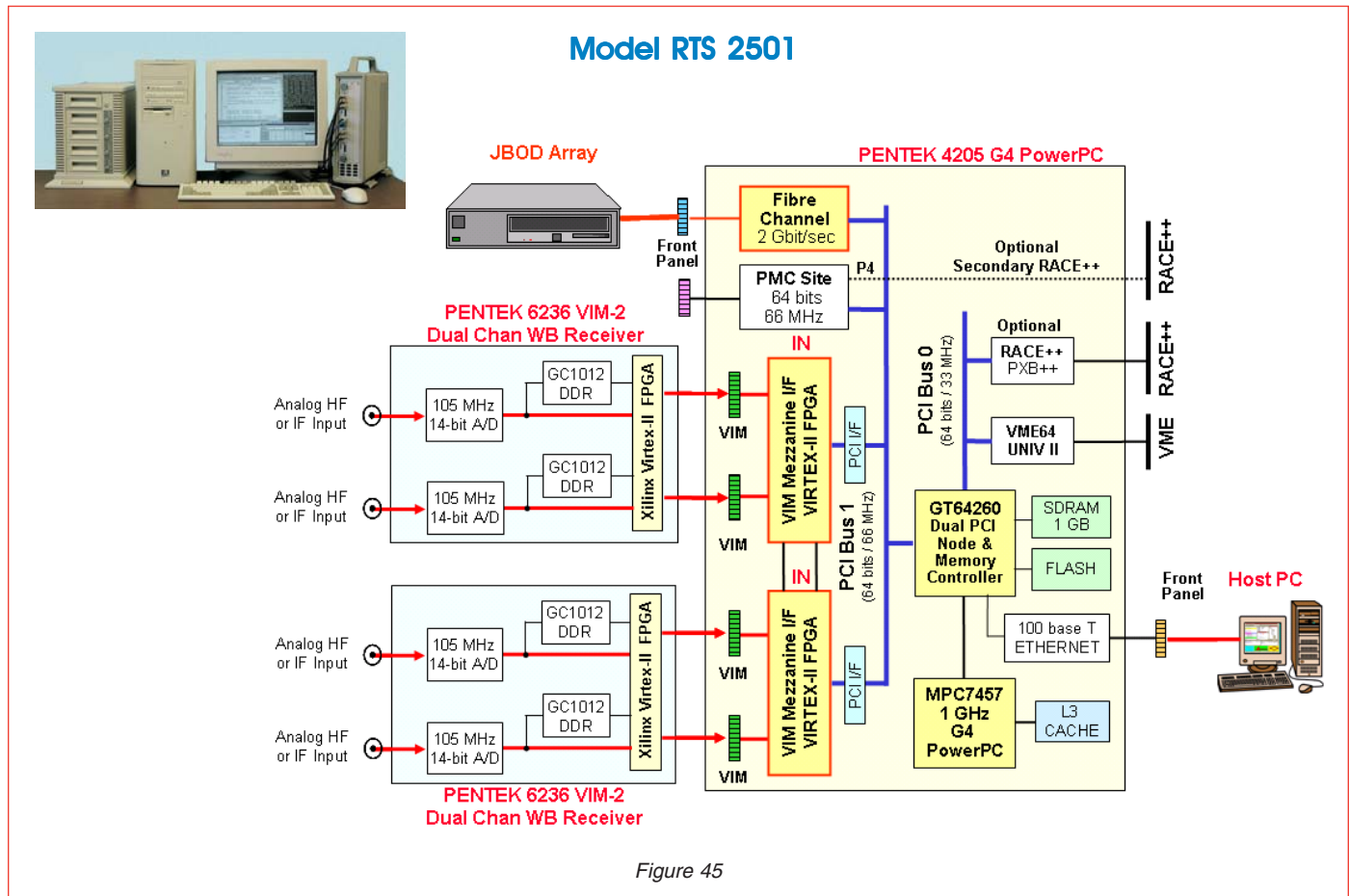
Core 430 DDC comes factory installed in the Model 7140-430. A multiplexer in front of the core allows data to be sourced from either A/D converter A or B. At the output, a multiplexer allows the 7140 to route either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any interger value between 1 and 4096. A TI DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 40 MHz.

Core 430 is also available for the Models 7240, 7340 and 7640.

## Systems

### Real-Time Wideband Signal Processing System



The Pentek RTS 2501 in Figure 45 is one of several highly-scalable, real-time platforms for acquiring, down-converting, processing, and recording wideband signals.

The heart of the RTS 2501 is the Pentek Model 4205 I/O Processor featuring a 1 GHz MPC7457 G4 PowerPC, mezzanine sites for both VIM and PMC modules, and two Xilinx Virtex-II FPGAs. The G4 PowerPC acts both as an executive for managing data transfer tasks as well as performing digital signal processing or formatting functions.

Attached to the 4205 I/O Processor are two Model 6236 Dual Channel A/D and Wideband Receiver VIM modules, each with two 14-bit 105 MHz A/D converters, two TI/GC1012B wideband digital downconverters and a Virtex-II FPGA.

A built-in Fibre Channel interface connects directly to JBOD or RAID hard disks for real time storage at rates up to 100 MB/sec. Optional RACE++ interfaces provide excellent I/O connectivity without sacrificing any of the mezzanine sites. Standard RS-232 and 100 base T Ethernet ports allow the PowerPC to communicate with a wide range of host workstations for control and software development applications.

Scalable from 2 to 80 channels in a single 6U VMEbus chassis, the RTS 2501 serves equally well as a development platform for advanced research projects and proof-of-concept prototypes, or as a cost-effective strategy for deploying high-performance, multichannel embedded systems.

More information on RTS systems on [pentek.com](http://pentek.com).

## Systems

### Real-Time Wideband Signal Processing and Recording System



Model RTS 2502

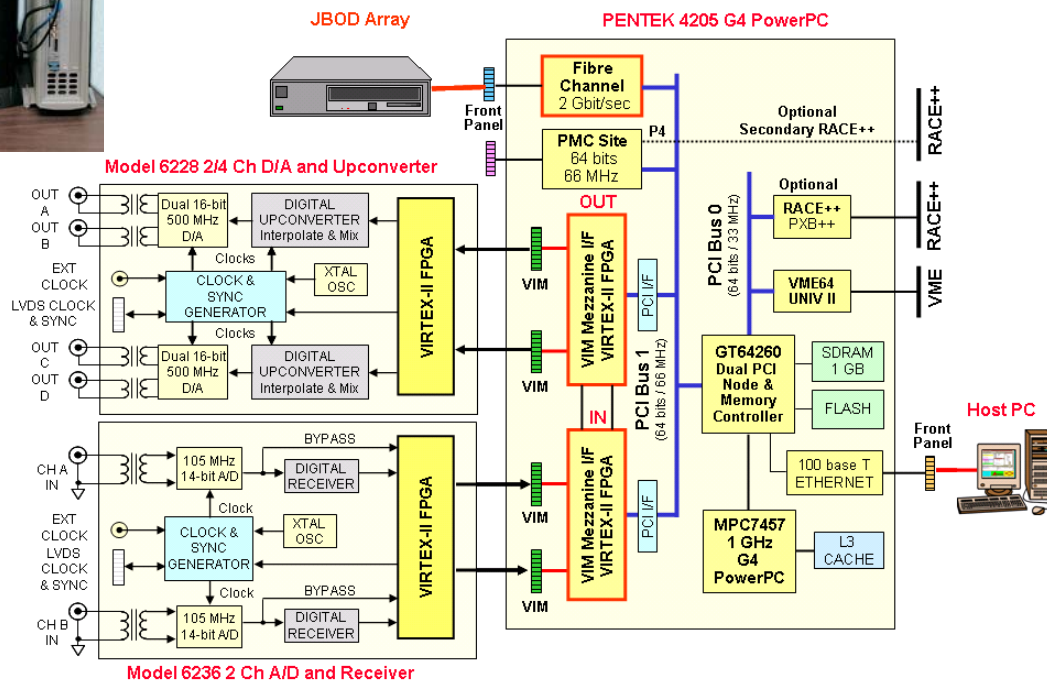


Figure 46

The Pentek RTS 2502 in Figure 46 is also a highly-scalable, real-time platforms for acquiring, downconverting, processing, and recording wideband signals.

The heart of the RTS 2502 is the Pentek Model 4205 I/O Processor featuring a 1 GHz MPC7457 G4 PowerPC, mezzanine sites for both VIM and PMC modules, and two Xilinx Virtex-II FPGAs. The G4 PowerPC acts both as an executive for managing data transfer tasks as well as performing digital signal processing or formatting functions.

Attached to the 4205 I/O Processor is a Model 6236 Dual Channel A/D and Wideband Receiver VIM module with two 14-bit 105 MHz A/D converters, two TI/GC1012B wideband digital downconverters and a Virtex-II FPGA.

Also attached to the 4205 processor is a Model 6228 4-channel 16-bit 500 MHz D/A with digital upconverters and a Virtex-II FPGA. The 6228 provides a path for analog playback of recorded signals or for real-time transmission of signals received by the 6236.

A built-in Fibre Channel interface connects directly to JBOD or RAID hard disks for real time storage at rates up to 100 MB/sec. Optional RACE++ interfaces provide excellent I/O connectivity without sacrificing any of the mezzanine sites. Standard RS-232 and 100 base T Ethernet ports allow the PowerPC to communicate with a wide range of host workstations for control and software development applications.

More information on RTS systems on [pentek.com](http://pentek.com).



## Systems

### Real-Time Wideband Signal Processing System



**Model RTS 2503**

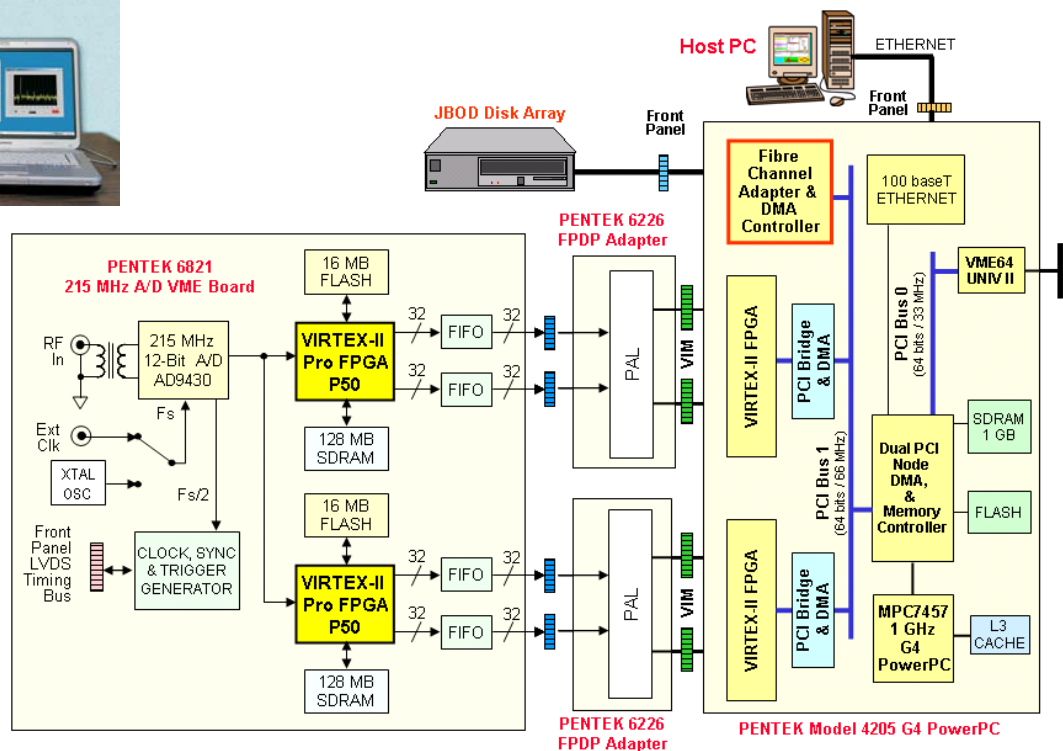


Figure 47

The Pentek RTS 2503 in Figure 47 extends the range of highly-scalable, real-time platforms for acquiring, downconverting, processing, and recording wideband signals to 215 MHz sampling frequency, by utilizing the single-channel Model 6821 or the dual channel Model 6822 215 MHz, 12-bit A/D converters. These attach to the Model 4205 I/O Processor with two Pentek Model 6226 FPDP Adapter VIM-2 modules. This system occupies two VMEbus slots.

Again, the heart of the RTS 2503 is the Pentek Model 4205 I/O Processor featuring a 1 GHz MPC7457 G4 PowerPC, mezzanine sites for both VIM and PMC modules, and two Xilinx Virtex-II FPGAs. The G4 PowerPC acts both as an executive for managing data transfer tasks as well as performing digital signal processing or formatting functions.

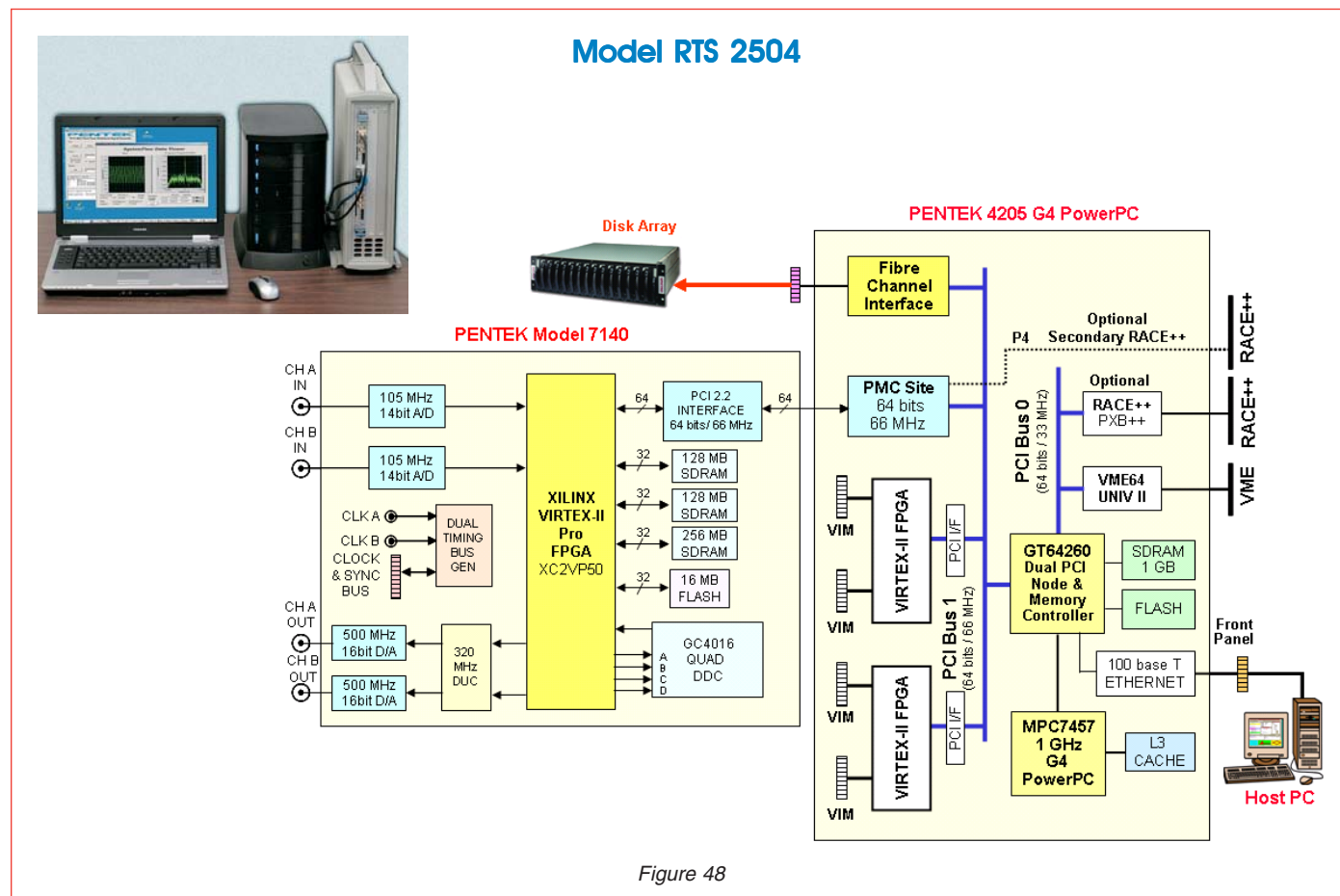
The built-in Fibre Channel interface connects directly to JBOD or RAID hard disks for real time storage at rates up to 100 MB/sec. Optional RACE++ interfaces provide excellent I/O connectivity without sacrificing any of the mezzanine sites. Standard RS-232 and 100 base T Ethernet ports allow the PowerPC to communicate with a wide range of host workstations for control and software development applications.

Scalable from 1 to 20 channels in a single 6U VMEbus chassis, the RTS 2503 allows the design engineer to take advantage of the latest technology for research projects and proof-of-concept prototypes, or as a cost-effective strategy for deploying high-performance, multichannel embedded systems.

More information on RTS systems on [pentek.com](http://pentek.com).

## Systems

### Real-Time Wideband Signal Processing and Recording System



The Pentek RTS 2504 in Figure 48 is similar to the System RTS 2502, except that the Models 6236 and 6228 have been replaced by the Model 7140 Transceiver PMC module described on page 36. The Model 7140 combines the downconverters and upconverters of these two models in one PMC/XMC module. Except for this change, the system performance and characteristics are identical.

Again, the heart of the RTS 2504 is the Pentek Model 4205 I/O Processor featuring a 1 GHz MPC7457 G4 PowerPC, mezzanine sites for both VIM and PMC modules, and two Xilinx Virtex-II FPGAs. The G4 PowerPC acts both as an executive for managing data transfer tasks as well as performing digital signal processing or formatting functions.

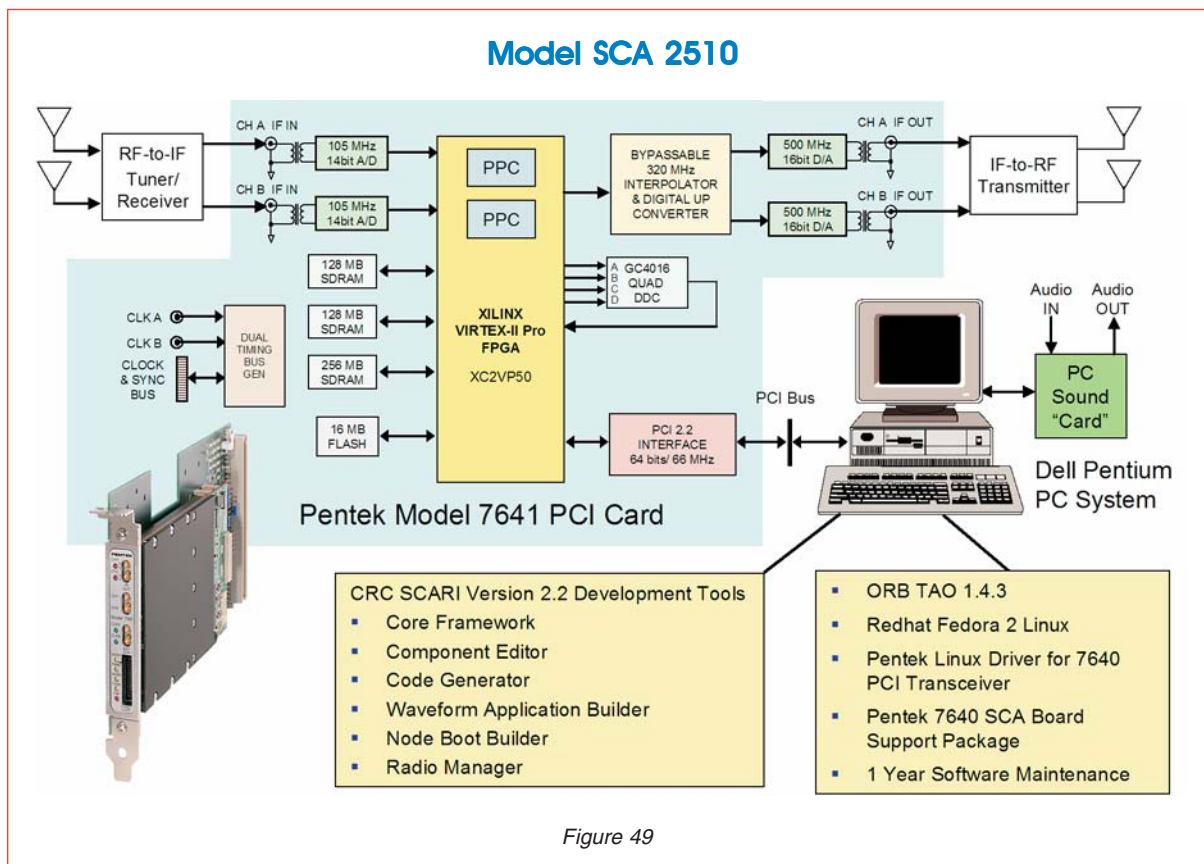
A built-in Fibre Channel interface connects directly to JBOD or RAID hard disks for real time storage at rates up to 100 MB/sec. Optional RACE++ interfaces provide excellent I/O connectivity without sacrificing any of the mezzanine sites. Standard RS-232 and 100 base T Ethernet ports allow the PowerPC to communicate with a wide range of host workstations for control and software development applications.

Scalable from 1 to 40 channels in a single 6U VMEbus chassis, the RTS 2504 serves equally well as a development platform for advanced research projects and proof-of-concept prototypes, or as a cost-effective strategy for deploying high-performance, multichannel embedded systems.

More information on RTS systems on [pentek.com](http://pentek.com).

## Systems

### SCA-Compliant Software Defined Radio Development System



The Pentek SCA 2510 Development Platform shown in Figure 49, is a complete low-cost system for developing software defined radio products.

The 7640 transceiver PCI board that we discussed on pages 36 and 37, ported with all the necessary SCA infrastructure, creates an SCA-compliant platform. Comprised of hardware and software components compatible with the SCA standard, the SCA 2510 platform is a PC-based system that runs under Linux.

The system includes an installed CRC SCARI++ core framework, Component Development Library and SDR development tools, plus the Pentek SCA board support package for the model 7640 and all the board-specific components.

This complete platform satisfies SCA requirements by offering a low-cost solution suitable for waveform developers, application developers and system integrators.

To support scalability to large platforms, an additional 7640 PCI card can be installed right in the PC motherboard. Furthermore, the identical board architecture is available in a PMC form factor, or a 3U or a 6U CompactPCI form factor that can be convection-cooled, ruggedized, or conduction-cooled.

These are all extremely appropriate for large deployed multichannel military systems. Future SCA system development based on these additional form factors is planned.

## Products

### DSP Boards for VMEbus

- Freescale AltiVec G4 PowerPC
- Texas Instruments C6000 DSPs
- Single, Dual, Quad and Octal Processor versions
- PMC, VIM, PCI and cPCI Mezzanines
- RACEway, RACE++, FPD and Fibre Channel Interfaces

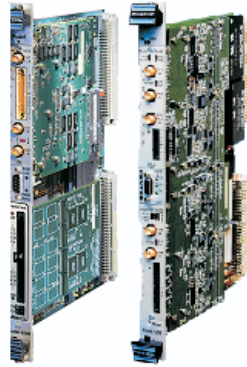


Figure 50

Pentek offers a comprehensive array of VMEbus DSP boards featuring the TMS320C6000 family of processor products from Texas Instruments and the AltiVec G4 PowerPC from Freescale.

On-board processor densities range from one to eight DSPs with many different memory and interface options available.

The Model 4290/91/92/93 series of VIM quad processor boards features the Texas Instruments latest TMS320C6000 family of fixed and floating point DSPs that represent a 10-fold increase in processing power over previous designs.

The Models 4294 and 4295 VIM processor boards feature four MPC74xx G4 PowerPC processors utilizing the AltiVec vector processor capable of delivering several GFLOPS of processing power.

The Model 4205 G4 PowerPC I/O processor board accepts both VIM and PMC mezzanines and includes built-in dual RACE++ interfaces plus Fibre Channel.

Once again, the ability of the system designer to freely choose the most appropriate DSP processor for each digital receiver application, facilitates system requirement changes and performance upgrades.

Full software development tools are available for workstations running Windows, Solaris, and Linux with many different development system configurations available.

### Summary

#### Benefits of Digital Receivers:

- Reduction of DSP processing demands
- Very fast tuning - No PLL'S
- Fast bandwidth selection
- Zero frequency drift and error
- Precise, stable filter characteristics
- Excellent dynamic range

To summarize, we first restate the major benefit of digital receivers:

*Digital receivers can dramatically reduce the DSP requirements for systems which need to process signals contained within a certain frequency band of a wideband signal.*

The fast tuning of the digital local oscillator and the easy bandwidth selection in the decimating digital filter make the digital receiver easy to control.

Since all of the circuitry uses digital signal processing, the characteristics are precise, predictable, and will not drift with time, temperature or aging. This also means excellent channel-to-channel matching and no need for calibration, alignment or maintenance.

With the addition of FPGA technology, dramatic increases in system density have been coupled with a significantly lower cost per channel. Furthermore, FPGA technology allows users to incorporate custom algorithms right at the front end of these systems.

As we have seen, there are inherently many benefits and advantages to you when using digital receivers. We hope that this introduction to digital receivers has been informative. We stand ready to discuss your requirements and help you configure a complete digital receiver system.

For all the latest information about Pentek's digital receivers, DSP boards and data acquisition products, be sure to visit Pentek's comprehensive website regularly at [pentek.com](http://pentek.com).



## Links



The following live links provide you with additional information about the Pentek Products and Systems presented in this handbook. **Just click on the Model number.** Live links are also provided to other handbooks or brochures that may be of interest in your software radio development projects.

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| <b>Handbooks &amp; Brochures</b> |  |      |
| Click here                       | Putting FPGAs to Work for Software Radio                               |      |
| Click here                       | Critical Techniques for High-Speed A/D Converters in Real-Time Systems |      |
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